CALIFORNIA INSTITUTE OF TECHNOLOGY
PHYSICS MATHEMATICS AND ASTRONOMY DIVISION

Sophomore Physics Laboratory

Physics 5 and 105 Course

Laboratory Notes

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Chapter 1

Alternating Current Network Theory

In this chapter we will study the properties of electronic networks propagating sinusoidal voltages and currents (alternate current/AC regime). In other words, voltage or current sources connected to the networks produce electromagnetic waves whose frequency can be ideally changed from 0 to ∞.

Considering an electromagnetic wave whose frequency f is 1MHz, (typical maximum frequency f used in this course of analog electronics) and the electromagnetic field propagates at a speed $c = 3 \cdot 10^8$m/s (1′/ns), the wavelength $\lambda = c/f$ will be usually much greater than several hundred feet, hundreds to thousands of times greater than the physical sizes of our electronic circuits. Consequently, each individual circuit component will have at any instant, to a high degree of accuracy, zero net total current flowing in or out of all its connections. Such an element is known as a *lumped element*.

When fields wavelength becomes comparable to the size of the circuit components, fields and currents can vary across the element, making it a *distributed element*. Examples of distributed elements include antennas, microwave waveguides, and the electrical power distribution grid.

For two-terminal lumped elements, we can conclude that at any instant, the current flowing out of one terminal must equal the current flowing into the other, so we can simply refer to the current flowing through the element and the potential difference (voltage difference or voltage drop) between the two terminals.

The AC analysis of such circuits is valid once the network is at the steady state, i.e. when the transient behavior (such as those ones produced by closing or opening switches) is extinguished.

In general, if we have a sinusoidal signal (sinusoidal voltages, or currents) applied to a circuit having at least one input and one output, we will expect a change in the amplitude and phase at the output. The determination of these quantities for quite simple circuits can be very complex. It is indeed important to develop a convenient representation of sinusoidal signals to simplify the analysis of circuits in the AC regime.

1.1 Symbolic Representation of a Sinusoidal Signals, Phasors

A sinusoidal quantity (a sinusoidal current or voltage for example) ,

$$A(t) = A_0 \sin(\omega t + \varphi),$$

is univocally characterized by the amplitude A_0, the angular frequency ω, and the initial phase φ. The phase φ corresponds to a given time shift t^* of the sinusoid ($\omega t^* = \varphi \Rightarrow t^* = \varphi/\omega$).

We can indeed associate to $A(t)$ an applied vector $\vec{A}$ in the complex plane with modulus $|A| = A_0 \geq 0$, rotating counter-clockwise around the origin O with angular frequency ω and initial angle φ (see figure 1.1). Such vectors are called *phasors.*

The complex representation of the phasor is[1]

$$\vec{A} = A_0 e^{j(\omega t + \varphi)}, \qquad j = \sqrt{-1},$$

or

$$\vec{A} = x + jy, \qquad \begin{cases} x = A_0 \cos(\omega t + \varphi) \\ y = A_0 \sin(\omega t + \varphi) \end{cases}$$

Extracting the real and the imaginary part of the phasor, we can easily compute its amplitude A_0 and phase φ, i.e.

$$|A| = \sqrt{\Re[\vec{A}]^2 + \Im[\vec{A}]^2} \qquad \varphi = \arg[A] = \arctan\left(\frac{\Im[\vec{A}]}{\Re[\vec{A}]}\right) \quad (t = 0),$$

[1] To avoid confusion with the electric current symbol i, it is convenient to use the symbol j for the imaginary unit.

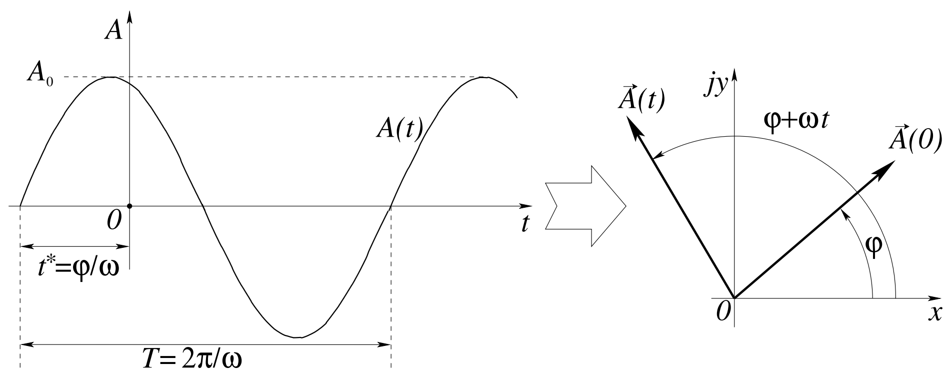


Figure 1.1: Sinusoidal quantity$A(t)$ and its phasor representation $\vec{A}$ at the initial time $t = 0$ and at time t.

and reconstruct the real sinusoidal quantity. It is worth noting that in general, amplitude A_0 and phase φ are functions of the frequency.

The convenience of this representation will be evident, once we consider the operation of derivation and integration of a phasor.

1.1.1 Derivative of a Phasor

Computing the derivative of a phasor $\vec{A}$, we get

$$\frac{d\vec{A}}{dt} = j\omega A_0 e^{j(\omega t+\varphi)} = j\omega \vec{A},$$

i.e. the derivative of a phasor is equal to the phasor times $j\omega$.

1.1.2 Integral of a Phasor

The integral of a phasor $\vec{A}$ is

$$\int_{t_0}^{t} \vec{A} dt' = \frac{1}{j\omega} \left[A_0 e^{j(\omega t+\varphi)} - A_0 e^{j(\omega t_0+\varphi)} \right] = \frac{1}{j\omega} \vec{A} + \text{const.},$$

i.e. the integral of a phasor is equal to the phasor divided by $j\omega$ plus a constant. For the AC regime we can assume the constant to be equal to zero without loss of generality.

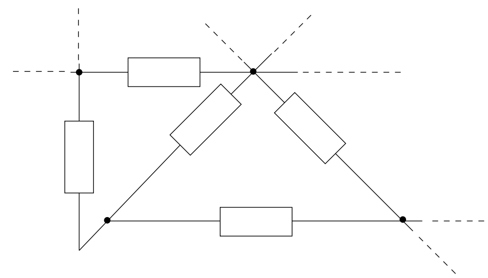


Figure 1.2: Generic representation of a network

1.2 Network Definitions

To make easier the understanding of network basic theorems, some more or less intuitive definitions must be stated.

An *electronic network* or circuit is a set of electronic components/devices connected together to modify and transmit/transfer energy/information. This information is generally called *an electric signal* or simply a signal.

To graphically represent a network, we use a set of coded symbols with terminals for the *network lumped elements* and lines for connections. These lines propagate the signal among the elements without changing it. The elements change the propagation of the electric signals.

A *network node* is a point where more than two network lines connect.

A *network loop, or mesh,* is any closed network line. To determine a mesh it is sufficient to start from any point of the circuit and come back running trough the network to the same point without passing through the same point.

Quantities defining signal propagation are voltages V across the elements and currents I flowing through them.

Solving an electronic network means determining the currents or the voltages of each point of it.

Figure 1.2 shows a generic portion of a network with 4 visible nodes, and 3 visible meshes. The empty boxes are the electronic elements of the network and their size is just for convenience and don't correspond to any physical dimensions. These are the points in the network where voltages and currents are modified.

1.2.1 Series and Parallel

Let's consider the two different connection topologies shown in figure 1.3, the parallel and the series connections.

A set of components is said to be in series if the current flowing through them and anywhere in the circuit is the same .

A set of components is said to be in parallel if the voltage difference between them is the same.

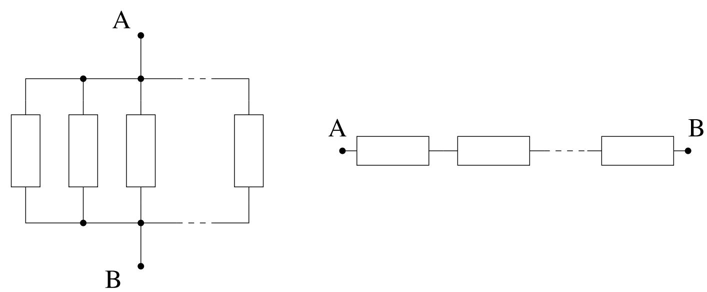


Figure 1.3: Considering the points A, and B, the components of the left circuit are in parallel, and those in the right circuit are in series.

1.2.2 Active and Passive Components

Circuit components can be divided into two categories: active and passive components. Active components are those devices that feed energy into the network. Voltage and current sources are active components. Amplifiers are also active components.

Passive components are those components, that do not feed energy to the network. Resistors, capacitors, inductors are typical passive components.

In general, both active and passive components dissipate energy.

1.3 Kirchhoff's Laws

Kirchhoff's laws, are fundamental for the solution of an electronic circuit. They can be derived from Maxwell's equations in the approximation of slowly varying field.

Kirchhoff's Voltage Law (KVL): The algebraic sum of the voltage difference v_k at the time t around a loop must be equal to zero at all times, i.e.

$$\sum_k v_k(t) = 0$$

Kirchhoff's Current Law(KCL): The algebraic sum of the currents i_k at the time t entering and leaving a node must be equal to zero at all times, i.e.

$$\sum_k i_k(t) = 0.$$

These laws hold for phasors as well.

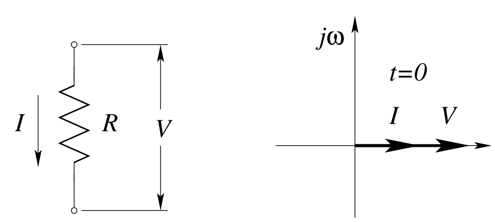
1.4 Passive Ideal Components with Phasors

Let's rewrite the I-V characteristic for the passive ideal components using the phasor notation. For sake of simplicity, we remove the arrow above the phasor symbol. To avoid ambiguity, we will use upper case letters to indicate phasors, and lower case letters to indicate a generic time dependent signal.

1.4.1 The Resistor

For time dependent signals, Ohm's law for a resistor with resistance R is

$$v(t) = Ri(t).$$



Introducing the phasor $I = I_0 e^{j\omega t}$ (see figure above), we get

$$v(t) = RI_0 e^{j\omega t},$$

and in the phasor notation

$$V = R\,I.$$

The frequency and time dependence are implicitly contained in the phasor current I.

1.4.2 The Capacitor

The variation of the voltage difference dv across a capacitor with capacitance C due to the amount of charge dQ, is

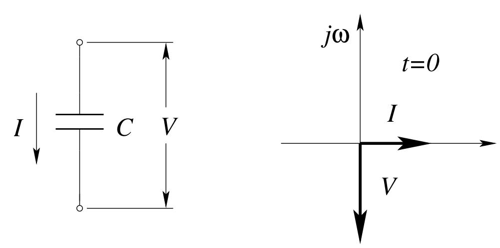
$$dv = \frac{dQ}{C}.$$

If the variation happens in a time dt and

$$i(t) = \frac{dQ}{dt},$$

we will have

$$\frac{dv(t)}{dt} = \frac{1}{C} i(t), \quad \Rightarrow \quad v(t) = \frac{1}{C}\int_0^t i(t')dt' + v(0).$$



For sinusoidal time dependence , we introduce the phasor $I = I_0 e^{j\omega t}$ (see figure above), and get

$$v(t) = \frac{1}{C}\int_0^t I_0 e^{j\omega t'} dt' + v(0),$$

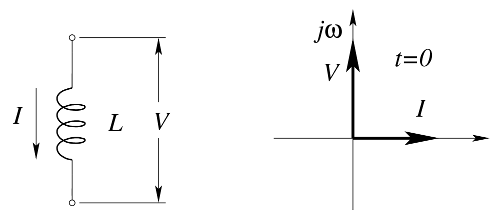
Using the phasor notation and supposing that for $t = 0$ the capacitor is discharged, we finally get

$$V = \frac{1}{j\omega C}\, I, \qquad , v(0) = 0.$$

1.4.3 The Inductor

The induced voltage $v(t)$ of an inductor with inductance L, is

$$v(t) = L\frac{di(t)}{dt}.$$



Introducing the phasor $I = I_0 e^{j\omega t}$ (see figure above), we get

$$v(t) = L\frac{d}{dt}I_0 e^{j\omega t},$$

and in the phasor notation

$$V = j\omega L\, I.$$

1.5 The Impedance and Admittance Concept

Let's consider a generic circuit with a port, whose voltage difference and current are respectively the phasors $V = V_0 e^{j(\omega t+\varphi)}$, and $I = I_0 e^{j(\omega t+\psi)}$. The ratio Z between the voltage difference and the current

$$Z(\omega) = \frac{V}{I} = \frac{V_0}{I_0}e^{j(\varphi-\psi)}.$$

is said to be the *impedance of the circuit.*

The inverse

$$Y(\omega) = \frac{1}{Z(\omega)}$$

is called the *admittance of the circuit.*

For example, considering the results of the previous subsection, the impedance of a resistor, a capacitor, and an inductor are respectively

$$Z_R = R, \qquad Z_C(\omega) = \frac{1}{j\omega C}, \qquad Z_L(\omega) = j\omega L,$$

and the admittances are

$$Y_R = \frac{1}{R}, \qquad Y_C(\omega) = j\omega C, \qquad Y_L(\omega) = \frac{1}{j\omega L}.$$

In general, the impedance or admittance of a circuit port is a complex function, which depends on the angular frequency ω. Quite often they are graphically represented by plotting the magnitude$|Z(\omega)|$or $|Y(\omega)|$in a double logarithmic scale and the phase $\arg[Z(\omega)]$or $\arg[Y(\omega)]$ in a logarithmic scale.

For completeness let´ s introduce some other definitions:

- The real part of the impedance $Z(\omega)$ is called *resistance*.
- The imaginary part of the impedance $Z(\omega)$ is called *reactance*.
- The real part of the admittance $Y(\omega)$ is called *conductance*.
- The imaginary part of the admittance $Y(\omega)$ is called *susceptance*.

1.5.1 Impedance in Parallel and Series

It can be easily demonstrated that the same laws for the total resistance of a series or a parallel of resistors hold for the impedance

$$Z_{tot} = Z_1 + Z_2 + ... + Z_N, \quad \text{(impedances in series)}$$

$$\frac{1}{Z_{tot}} = \frac{1}{Z_1} + \frac{1}{Z_1} + ... + \frac{1}{Z_N}, \quad \text{(impedances in parallel)}$$

It is left as exercise to derive the homologue laws for the admittance.

1.5.2 Ohm's Law for Sinusoidal Regime

Thanks to the impedance concept, we can generalize Ohm's law and write the fundamental equation (*Ohm's law for sinusoidal regimes*)

$$V(\omega) = Z(\omega)I(\omega).$$

1.6 Two-Port Networks

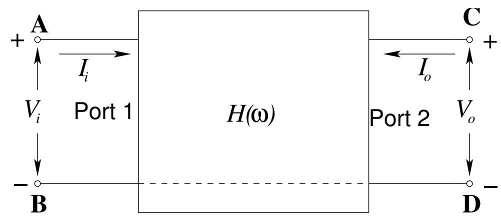


Figure 1.4: Two-port network circuit representation with terminals **B** and **D** connected. The voltage difference signs and current directions are conventional.

A linear circuit with one pair of input terminals **A, B** and one pair output terminals **C, D** is called *two-port network* (see figure 1.4). The electronic circuits we will consider here, are two-port network with terminals **B** and **C** connected together**[2].** In this case, to completely characterize the behavior of a two-port network, we can study the response of the output V_o as a function of the angular frequency ω of a sinusoidal input V_i.

In general, we can write

$$V_o(\omega) = H(\omega)V_i(\omega), \quad \text{or} \quad H(\omega) = \frac{V_o(\omega)}{V_i(\omega)},$$

where the complex function $H(\omega)$ is called the *transfer function or frequency response of the two-port network*. The transfer function contains the information of how the amplitude and the phase of the input changes when it reaches the output. Knowing the transfer function of this particular two-port network, we characterize the circuit[2]. The definition of $H(\omega)$ suggests a way of measuring the transfer function. In fact, exciting the input with a sinusoidal wave, we can measure at the output the amplitude and the phase lead or lag respect to the input signal.

[2] A deeper understanding of the transfer function of a circuit requires the concept of the Fourier transform and the Laplace transform and the convolution theorem. See [2] appendix C

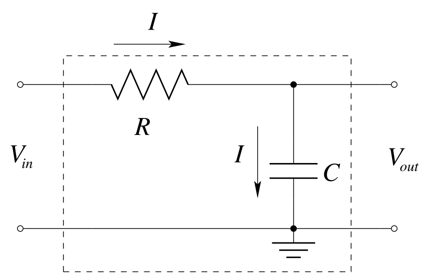


Figure 1.5: RC low-pass filter circuit.

1.6.1 Bode Diagrams

To graphically represent $H(\omega)$, it is common practice to plot the magnitude $|H(\omega)|$ (gain) in a double logarithmic scale, and the phase $\arg[H(\omega)]$ using a logarithmic scale for the angular frequency. These plots are called Bode diagrams. Units for ω are normally rad/s or Hz. The magnitude is quite often expressed in decibels dB (see appendix C)

$$X\text{dB} = 20\log_{10} X$$

For example 20dB = 10, 40dB=100, etc... Practically, plotting a quantity in dB (which is not a units symbol such as m,s,kg, Ω) corresponds to plot the quantity on a logarithmic scale.

The phase can be expressed in radians (rad) or in degrees (deg).

Logarithmic scales have the advantage of emphasizing asymptotic trends and the disadvantage of flattening small variations. In other words, variations much smaller that the range of the plotted values become quite often indistinguishable in a logarithmic scale. To find out such kind of behavior, it is a good practice to look at magnitudes in both linear and logarithmic plots.

The Asymptotic Bode diagram [1], a simplification of the frequency response of a system is a convenient approximation of the characteristics of $H(\omega)$.

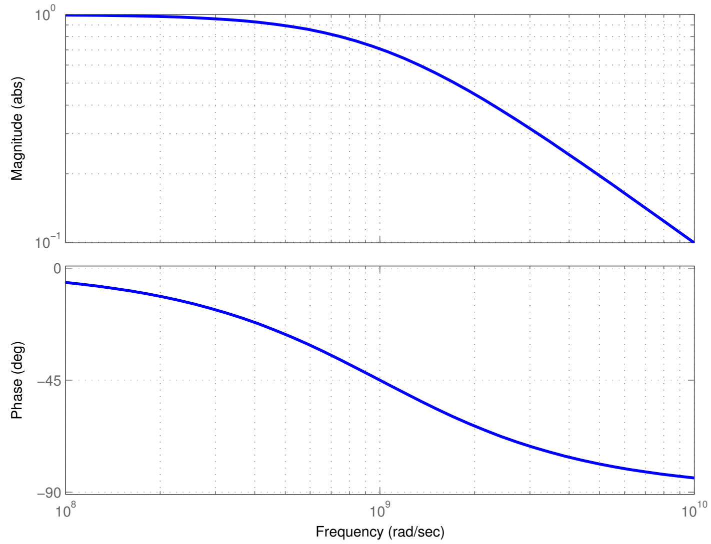


Figure 1.6: RC low-pass filter circuit transfer function.

1.6.2 The RC Low-Pass Filter

Figure 1.5 shows the *RC low-pass filter circuit*. The input and output voltage differences are respectively[3]

$$\begin{aligned} V_{in} &= Z_{in} I = \left(R + \frac{1}{j\omega C}\right) I, \\ V_{out} &= Z_{out} I = \frac{1}{j\omega C} I, \end{aligned}$$

and the transfer function is indeed

$$H(\omega) = \frac{V_{out}}{V_{in}} = \frac{1}{1 + j\tau\omega}, \qquad \tau = RC.$$

or

$$H(\omega) = \frac{1}{1 + j\omega/\omega_0}, \qquad \omega_0 = \frac{1}{RC}.$$

[3] V_{out} as function of V_{in} can be directly calculated using the voltage divider equation.

Computing the magnitude and phase of $H(\omega)$, we obtain

$$\begin{aligned} |H(\omega)| &= \frac{1}{\sqrt{1+\tau^2\omega^2}} \\ \arg(H(\omega)) &= -\arctan\left(\frac{\omega}{\omega_0}\right) \end{aligned}$$

Figure 1.6 shows the magnitude and phase of $H(\omega)$. The parameter τ and ω_0 are called respectively the *time constant* and *angular cut-off frequency of the circuit*. The cut-off frequency is the frequency where the output V_{out} is attenuated by a factor $1/\sqrt{2}$.

It is worthwhile to analyze the qualitative behavior of the capacitor voltage difference V_{out} at very low frequency and at very high frequency.

For very low frequency the capacitor is an open circuit and V_{out} is essentially equal to V_{in}. For high frequency the capacitor acts like a short circuit and V_{out} goes to zero.

The capacitor produces also a delay as shown in the phase plot. At very low frequency the V_{out} follows V_{in} (they have the same phase). The output V_{out} loses phase ($\omega t = \varphi \Rightarrow t = \varphi/\omega$) when the frequency increases. The output V_{out} starts lagging due to the negative phase φ, and then approaches a maximum delay at a phase shift of $-\pi/2$.

1.6.3 The RC High-Pass Filter

Figure 1.7 shows the *RC high-pass filter circuit*. The input and the output voltage differences are respectively

$$\begin{aligned} V_{in} &= Z_{in}I = \left(R + \frac{1}{j\omega C}\right) I, \\ V_{out} &= Z_{out}I = RI, \end{aligned}$$

and indeed the transfer function is

$$H(\omega) = \frac{V_{out}}{V_{in}} = \frac{j\omega\tau}{1+j\tau\omega}, \qquad \tau = RC.$$

or

$$H(\omega) = \frac{j\omega/\omega_0}{1+j\omega/\omega_0}, \qquad \omega_0 = \frac{1}{RC}.$$

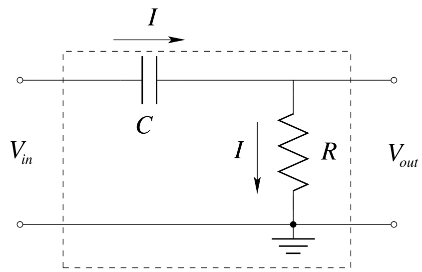


Figure 1.7: RC high-pass filter circuit

Computing the magnitude and phase of $H(\omega)$, we obtain

$$
\begin{aligned}
|H(\omega)| &= \frac{\tau\omega}{\sqrt{1+\tau^2\omega^2}}, \\
\arg(H(\omega)) &= \arctan\left(\frac{\omega_0}{\omega}\right)
\end{aligned}
$$

Figure 1.8 shows the magnitude and phase of $H(\omega)$. The definitions in the previous subsection, for τ and ω_0, hold for the RC high-pass filter.

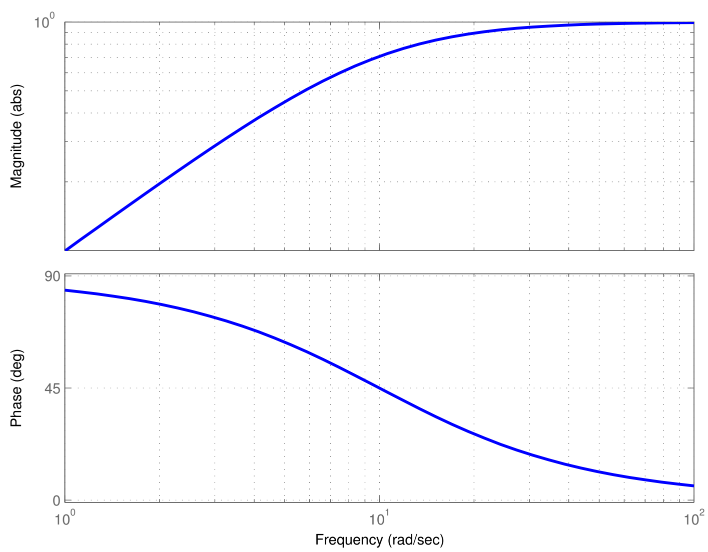


Figure 1.8: RC high-pass filter circuit transfer function.

1.7 Ideal Sources

1.7.1 Ideal Voltage Source

An ideal voltage source is a source able to deliver a given voltage difference V_s between its leads independent of the load R attached to it (see figure 1.9). It follows from Ohm's law that a voltage source is able to produce the current I necessary to keep constant the voltage difference V_s across the load R. The symbol for the ideal voltage source is shown in figure 1.9.

Quite often, a real voltage source exhibits a linear dependence on the resistive load R. It can be represented using an ideal voltage source V_s in series with a resistor R_s called input resistance of the source. Applying Ohm's law, it can be easily shown that the voltage and current through the load R are

$$V = \frac{R}{R + R_s} V_s, \qquad I = \frac{V_s}{R + R_s}.$$

If we assume

$$R \gg R_s, \quad \Rightarrow \quad V \simeq V_s, \quad I \simeq \frac{V_s}{R}.$$

Under the previous condition, the real voltage source approximates the ideal case.

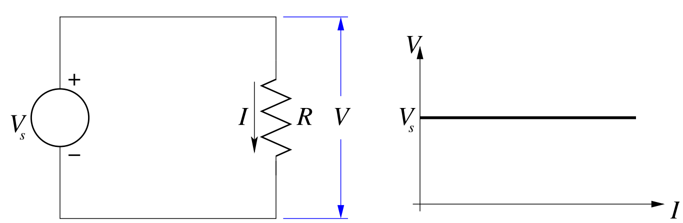


Figure 1.9: Ideal voltage source.

1.7.2 Ideal Current Source

An ideal current source is a source able to deliver a given current I_s that does not depend on the load R attached to it (see figure 1.10). It follows from Ohm's law that an ideal current source is able to produce the voltage difference V across the load R needed to keep I_s constant. The symbol for the ideal current source is shown in figure 1.10.

A real current source exhibits a dependence on the resistive load R, which can be represented using an ideal current source I_s in parallel with a resistor R_s. Applying Ohm's law and the KCL, it can be easily shown that the voltage and current through the load R are

$$I = \frac{R_s}{R + R_s} I_s, \qquad V = \frac{R_s R}{R_s + R} I_s.$$

If we suppose

$$R_s \gg R, \quad \Rightarrow \quad I \simeq I_s, \quad V \simeq R I_s \gg 0$$

Under the previous condition, the real current source approximates the ideal case.

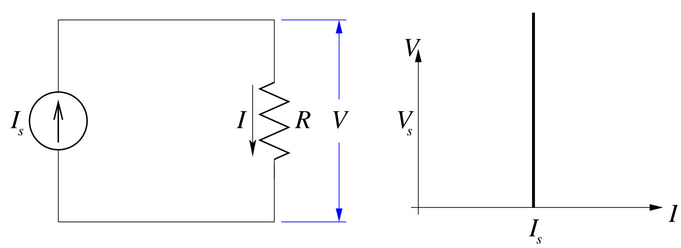


Figure 1.10: Ideal current source.

1.8 Equivalent Networks

Quite often, the analysis of a network becomes easier by replacing part of it with an equivalent and simpler network or dividing it into simpler subnetworks.

For example, the voltage divider is an equation easy to remember that allows to divide a complex circuit in two parts simplifying the search of the solution.

Thévenin and Norton theorems give us two methods to calculate equivalent circuits which behave like the original circuit, as seen from two points

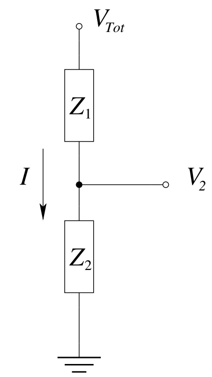


Figure 1.11: Voltage divider circuit.

of it. The techniques briefly explained in this section, will be then extensively used in the next chapters .

1.8.1 Voltage Divider

The voltage divider equation is applicable every time we have a circuit which can be re-conducted to a series of two simple or complex components. Considering the circuit branch of figure 1.11 and applying Ohm's law, we have

$$\begin{aligned} V_{Tot} &= (Z_1 + Z_2)I \\ V_2 &= Z_2 I \end{aligned}$$

and indeed

$$V_2 = \frac{Z_2}{Z_1 + Z_2} V_{Tot},$$

which is the voltage divider equation.

1.8.2 Thévenin Theorem

Thévenin theorem allows us to find an equivalent circuit for a network seen from two points **A** and **B** using an ideal voltage source V_{Th} in series with an impedance Z_{Th}.

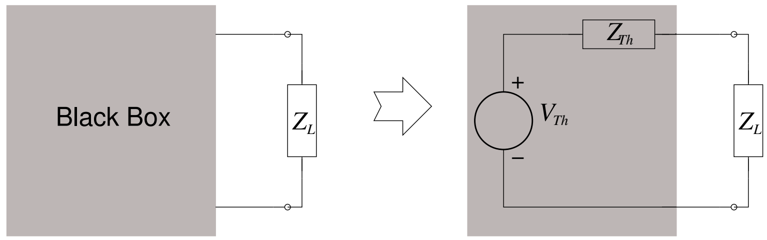


Figure 1.12: Thévenin equivalent circuit illustration.

The equivalence means that if we place a load Z_L between **A** and **B** in the original circuit (see figure 1.12) and measure the voltage V_L and the current I_L across the load, we will obtain exactly the same V_L and I_L if $Z_L$is placed in the equivalent circuit. This must be true for any load we connect between the points **A** and **B** .

The previous statement and the linearity of the circuit can be used to find V_{Th} and Z_{Th}. In fact, if we consider $Z_L = \infty$ (open circuit, OC), we will have

$$V_{Th} = V_{OC} \ .$$

The Voltage V_{Th} is just the voltage difference between the two leads **A** and **B**.

For $Z_L = 0$ (short circuit, SC) we must have

$$I_{SC} = \frac{V_{Th}}{Z_{Th}} = \frac{V_{OC}}{Z_{Th}} \ .$$

and therefore

$$Z_{Th} = \frac{V_{OC}}{I_{SC}} \ .$$

The last expression says that the Thévenin impedance is the impedance seen from the points **A** and **B** of the original circuit.

If the circuit is known, the Thévenin parameter can be calculated in the case for the terminals **A** and **B** open. In fact, V_{Th} is just the voltage across **A** and **B** of a known circuit. Replacing the ideal voltage sources with short circuits (their resistance is zero) and ideal current sources with open circuits (their resistance is infinite), we can calculate the impedance Z_{Th} seen from terminals **A** and **B**.

Considering the previous results, we can finally state Thévenin theorem as follows:

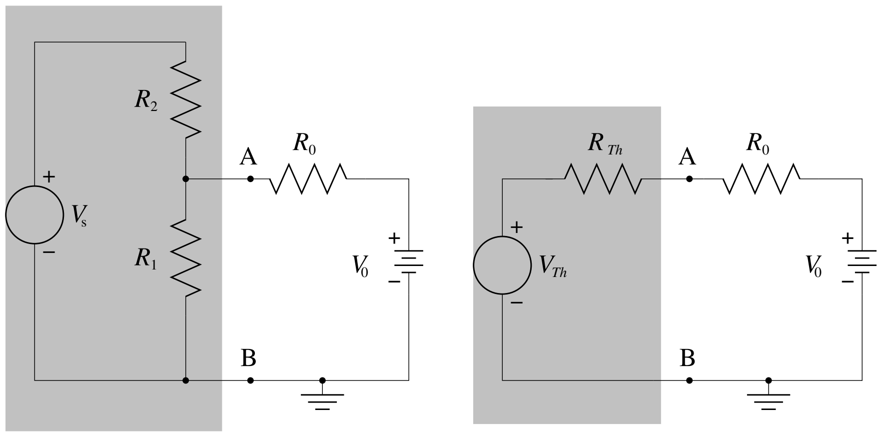


Figure 1.13: Thévenin equivalent circuit example

Any circuit seen from two points can be replaced by an ideal voltage source of voltage V_{Th} in series with impedance Z_{Th}. V_{Th} is the voltage difference between the two point of the original circuit. Z_{Th} is the impedance seen from these two points, short-circuiting all the ideal voltage generators and open-circuiting all the ideal current generators.

Example:

We want to find the Thévenin circuit of the network enclosed in the gray rectangle of figure 1.13. To find R_{Th}, and V_{Th} we have to disconnect the circuit in the points **A** and **B.** In this case, the voltage difference between these two points, thanks to the voltage divider equation, is

$$V_{Th} = \frac{R_1}{R_1 + R_2} V_s.$$

Short circuiting V_s we will have R_1 in parallel with R_2. The Thévenin resistance R_{Th} will be indeed

$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2}.$$

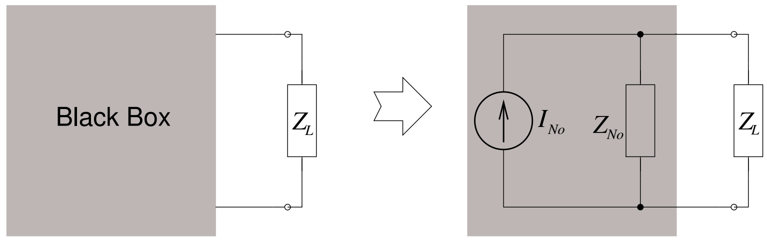


Figure 1.14: Norton equivalent circuit illustration.

1.8.3 Norton Theorem

*Any kind of active network seen from two points **A** and **B** can by replaced by an ideal current generator I_{No} in parallel with a impedance Z_{No}. The current I_{No} corresponds to the short-circuit current of the two points **A** and **B**. The Resistance Z_{No} is the Thévenin resistance $Z_{No} = Z_{Th}$.*

The proof of this theorem is left as exercise.

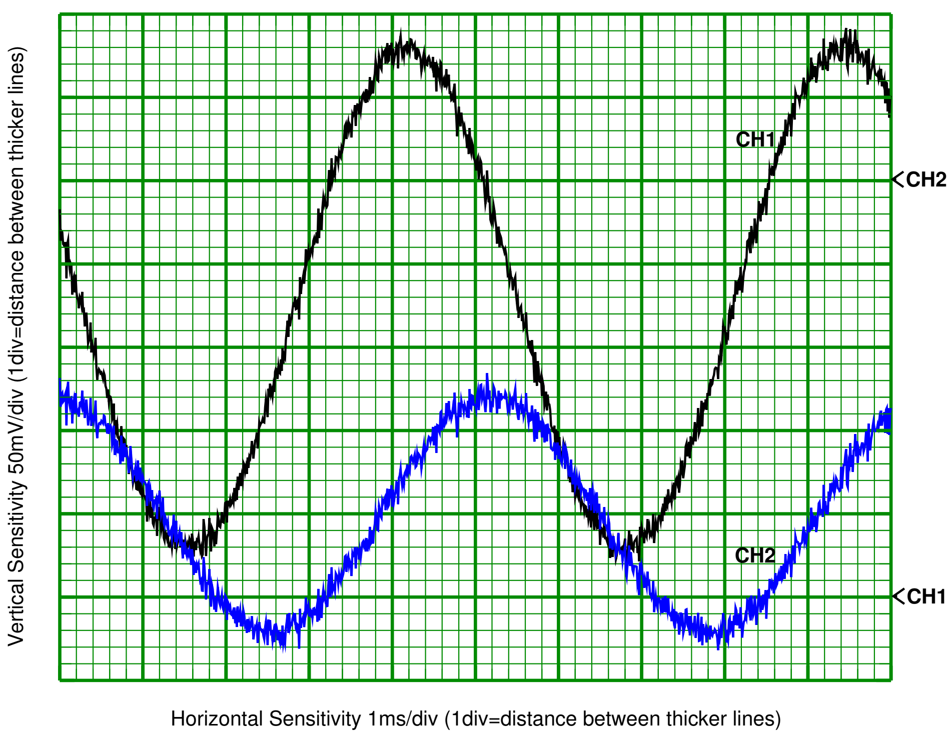
1.9 First Laboratory Week

This first laboratory class is essentially intended to help the student to become acquainted with the laboratory instrumentation (function generator, digital multimeter, circuit bread board, connectors), and with the use of passive components and their mathematical descriptions.

1.9.1 Pre-laboratory Problems

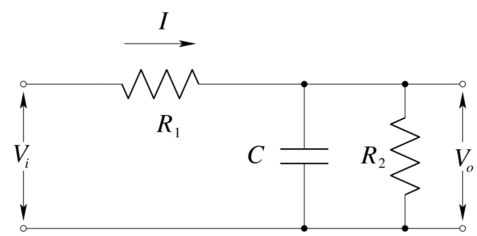
To complete the preparatory problems, it is recommended to read sections 1.1 to 1.6, and appendix E for the laboratory procedure.

1. Considering the figure below (a "snapshot" of an oscilloscope display), determine the peak to peak amplitude, the DC offset, the frequency of the two sinusoidal curves, and the phase shift between the two curves (channels horizontal axis position is indicated by an arrow and the channel name on the right of the figure).



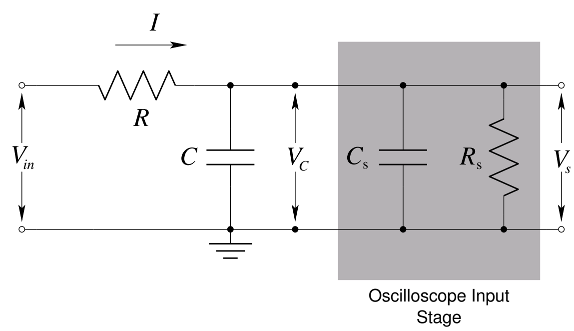
1. Sketch in a graph the magnitude and phase of the RC series circuit input impedance Z_i. Determine the two asymptotic behavior of $|Z_i|$,i.e. where the resistive and the capacitive behavior dominate.

2. Assuming that $R_2 \gg R_1$, repeat the previous problem for the following circuit



Hint: in this case there are three dominant behaviors, two resistive and one capacitive, and two frequencies which separate the three dominant behaviors.

3. The circuit below includes the impedance of the input channel of the CRT oscilloscope, and V_s is indeed the real voltage measured by the instrument.



Find the voltage $V_s(\omega)$, and the angular cut-off frequency ω_0 of the transfer function V_s/V_{in}(i.e. the value of ω for which $|V_s/V_{in}| = 1/\sqrt{2}$).
Show that for $\omega = 0$ the $V_s(\omega)$ formula simplifies and becomes the resistive voltage divider equation.
Demonstrate that the conditions to neglect the input impedance of the oscilloscope are the following :

$$C \gg C_s, \qquad R \ll R_s$$

(Hint: use the voltage divider equation to write V_C.)

4. Considering the previous circuit, calculate the value of R needed to obtain $V_{in} \simeq V_s$ with a fractional systematic error of 1%, if $\omega = 0$rad/s and $R_s = 1\text{M}\Omega$.

5. Determine the values of R, and C needed to get a RC series circuit cut-off frequency of 20kHz. Choose values which make the oscilloscope impedance negligible ($R_s = 1\text{M}\Omega$, $C_s = 25\text{pF}$).

1.9.2 Procedure

Whenever you work with electronic circuits as a beginner (all students are considered beginners; it doesn't matter which personal skills they already have), some extra precautions must be taken to avoid injuries. These are the main ones:

- NEVER CONNECT INSTRUMENT PROBES OR LEADS TO AN OUTLET OR MORE IN GENERAL TO THE POWER LINE.

- DO NOT TRY TO FIX/IMPROVE AN INSTRUMENT BY YOURSELF.

- DO NOT POWER AN INSTRUMENT WHICH IS NOT WORKING OR DISASSEMBLED.

- DO NOT TOUCH A DISASSEMBLED OR PARTIALLY DISASSEMBLED INSTRUMENT, EVEN IF IT IS NOT POWERED.

- WEAR PROTECTIVE GOGGLES EVERY TIME YOU USE A SOLDERING IRON.

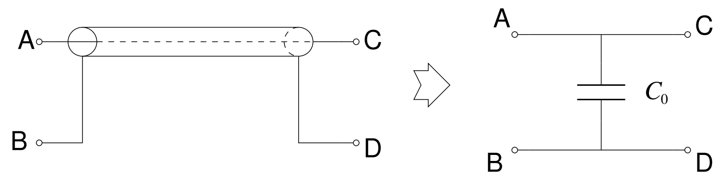
- TO AVOID EXPLOSIONS, NEVER USE A SOLDERING IRON ON A POWERED CIRCUIT AND BATTERIES.

- PLACE A FAN TO DISPERSE SOLDER VAPORS DURING SOLDERING WORK.

Read carefully the text before starting the laboratory measurements.

BNC cables and wires terminated with banana connectors are available to connect the circuit under measurement to the instruments.

BNC[4] cables, a diffused type of radio frequency (RF) coaxial shielded cable, have an intrinsic and quite well defined capacitance due to their geometry as shown in the figure below



They have typical linear density capacitance $\Delta C/\Delta l \simeq= 98$pF/m. Wires terminated with banana connectors have smaller capacitance than BNC cables but not as constant as BNC cables (Why?).

1. Build a RC low-pass or a RC high-pass filter with a cut-off frequency between 10kHz to 100kHz. Choose components values which make the perturbation of the input impedance of the oscilloscope negligible. Then, do the following

   (a) Verify the circuit transfer function, and in particular for frequencies $\nu \ll \nu_0$ and $\nu \gg \nu_0$

   (b) Find the cut-off frequency ν_o knowing the expected magnitude and phase values, and compare with the theoretical values

   (c) Change the capacitor value to be comparable to the oscilloscope input capacitance or the BNC cable capacitance and experimentally find the new cut-off frequency ν_1. Compare with the theoretical value.

   (d) Drive the circuit input with a square wave and verify the transient response of the circuit.

2. Measure the output impedance of the function generator for a given fixed sinusoidal frequency. Place at least three different loads to perform the measurement.

[4] "BNC" seems to stand for Bayonet Neill Concelman (named after Amphenol engineer Carl Concelman). Other sources claims that the acronym means British Navy Connector. What is certain is that the BNC connector was developed in the late 1940's as a miniature version of the type C connector (what does the "C" stand for ?)

Bibliography

[1] Ref for Maxwell equations versus Kirchhoff's laws.

[2] Microelectronics, Jacob Millman, and Arvin Grabel , Mac-Graw Hill

Chapter 2

Resonant Circuits

2.1 Introduction

Resonators, one of the most useful and used device, are essentially physical systems that present a more or less pronounced peak in the transfer function.

In general, their performance is measured by a dimensionless parameter named quality factor Q, which characterizes the sharpness of the resonant peak. The higher the quality factor the sharper is the peak and the better is the resonator.

Quite often, the major issues of building a resonator are to obtain very high quality factors and good stability. For example, mechanical oscillators made of fused silica fibers under load, can achieve quality factors above 10^8 in the acoustic band[**?**], and good stability if they are thermostabilized. Very high quality factors in electronics can be achieved using piezoelectric oscillator or quartz oscillators. Lasers and resonant cavities made of mirrors can be used to build resonators in the optical frequency range . The same principle can be applied in the microwave range. Thermal stabilization is always a key ingredient to obtain high stability.

Resonators made with electronic passive components, reaching quality factors values up to 10-100 or more, are quite easy to realize. In the next sections we will study two typical resonant circuits, the LCR series and LCR parallel circuits.

2.2 The LCR Series Resonant Circuit

Figure 2.1 shows the so called *LCR series resonant circuit*. Depending on voltage difference, we are considering as the circuit output (the capacitor, the resistor, or the inductor), this circuit shows a different behavior. Let's study indeed in the frequency domain, and the transient response of this passive circuit for each one of the output.

2.2.1 Frequency Response with Capacitor Voltage Difference as Circuit Output

Considering the voltage difference V_C across the capacitor the circuit output, we will have

$$\begin{aligned} V_{in} &= \left(R + j\omega L + \frac{1}{j\omega C} \right) I, \\ V_C &= \frac{1}{j\omega C} I \ , \end{aligned}$$

and the transfer function will be

$$H_C(\omega) = \frac{1}{j\omega RC - \omega^2 LC + 1}.$$

For sake of simplicity it is convenient to define the two following quantities

$$\omega_0^2 = \frac{1}{LC}, \qquad Q = \frac{1}{R}\sqrt{\frac{L}{C}} = \omega_0 \frac{L}{R}$$

The parameter Q is the quality factor of the circuit, and the angular frequency ω_0 is the resonant frequency of the circuit if $R = 0$.

Considering the previous definitions, and after some algebra, $H_C(\omega)$ becomes

$$H_C(\omega) = \frac{\omega_0^2}{\omega_0^2 - \omega^2 + j\omega \frac{\omega_0}{Q}} \ . \tag{2.1}$$

Computing the magnitude and phase of $H_C(\omega)$, we obtain

$$|H_C(\omega)| = \frac{\omega_0^2}{\sqrt{(\omega_0^2 - \omega^2)^2 + \left(\omega \frac{\omega_0}{Q}\right)^2}} \ ,$$

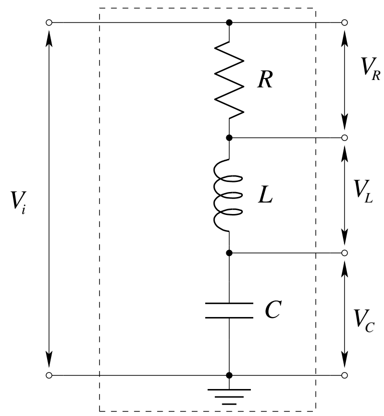


Figure 2.1: LCR series circuit.

$$\arg\left[H_C(\omega)\right] \;=\; -\arctan\left(\frac{1}{Q}\,\frac{\omega_0\omega}{\omega_0^2-\omega^2}\right)\,.$$

The magnitude has maximum for

$$\omega_C^2 = \omega_0^2\left(1-\frac{1}{2Q^2}\right)\,,$$

and the maximum is

$$|H_C(\omega_C)| = \frac{Q}{\sqrt{1-\frac{1}{4Q^2}}}\,.$$

If $Q \gg 1$ then $\omega_C \simeq \omega_0$, and $|H_C(\omega_C)| \simeq Q$.
Far from resonance ω_C, the approximate behavior of $|H_C(\omega)|$ is

$$\begin{aligned} \omega \;\ll\; \omega_C \qquad &\Rightarrow \qquad |H_C(\omega)| \simeq 1\,, \\ \omega \;\gg\; \omega_C \qquad &\Rightarrow \qquad |H_C(\omega)| \simeq \frac{\omega_0^2}{\omega^2}\,. \end{aligned}$$

Figure 2.2 shows the magnitude and phase of $H_C(\omega)$. In this case the circuit is a low pass filter of the second order because of the asymptotic slope $1/\omega^2$.

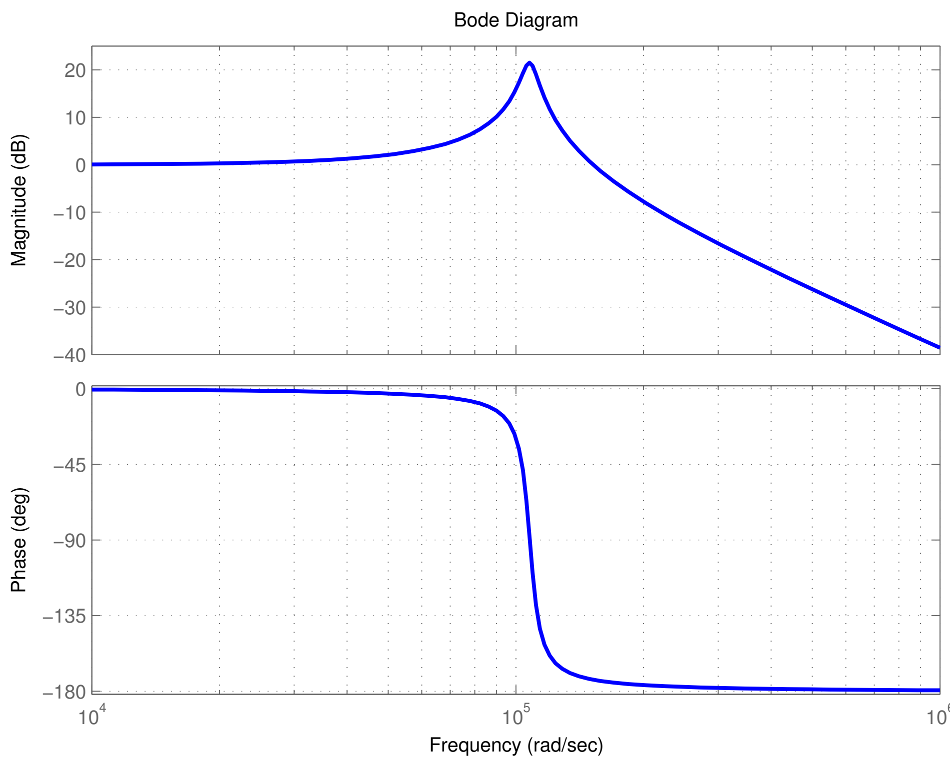


Figure 2.2: Transfer function $H_C(\omega)$ of the LCR series resonant circuit with a resonant angular frequency $\omega_C \simeq 10.7$krad/s.

2.2.2 Frequency Response with Inductor Voltage Difference as Circuit Output

Considering the voltage difference V_L across the inductor as the circuit output, we will have instead

$$H_L(\omega) = -\frac{\omega^2 LC}{j\omega RC - \omega^2 LC + 1}.$$

Using the definition of Q, and ω_0 and after some algebra, $H_L(\omega)$ becomes

$$H_L(\omega) = \frac{-\omega^2}{\omega_0^2 - \omega^2 + j\omega\frac{\omega_0}{Q}} \tag{2.2}$$

Computing the magnitude and phase of $H_L(\omega)$, we obtain

$$\begin{aligned} |H_L(\omega)| &= \frac{\omega^2}{\sqrt{(\omega_0^2-\omega^2)^2+\left(\omega\frac{\omega_0}{Q}\right)^2}} \\ \arg\left[H_L(\omega)\right] &= \arctan\left(\frac{1}{Q}\,\frac{\omega\omega_0}{\omega_0^2-\omega^2}\right) \end{aligned}$$

The magnitude has a maximum for

$$\omega_L^2 = \omega_0^2\,\frac{1}{1-\frac{1}{2Q^2}}\ ,$$

and the maximum is

$$|H_L(\omega_L)| = \frac{Q}{\sqrt{1-\frac{1}{4Q^2}}}.$$

If $Q \gg 1$ then $\omega_L \simeq \omega_0$, and $|H_L(\omega_L)| \simeq Q$.

Far from resonance ω_L, the approximate behavior of $|H_L(\omega)|$ is

$$\begin{aligned} \omega \ll \omega_L \quad &\Rightarrow \quad |H_L(\omega)| \simeq \frac{\omega^2}{\omega_0^2} \\ \omega \gg \omega_L \quad &\Rightarrow \quad |H_L(\omega)| \simeq 1 \end{aligned}$$

Figure 2.3 shows the magnitude and phase of $H_L(\omega)$. In this case the circuit is a second order high pass filter.

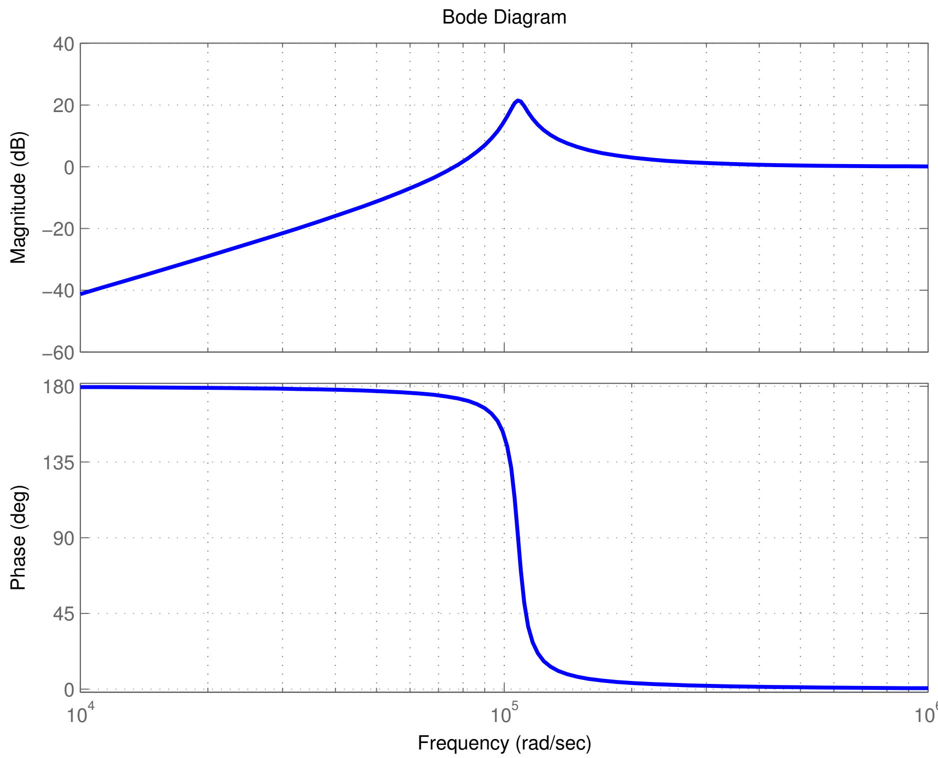


Figure 2.3: Transfer function $H_L(\omega)$ of the LCR series resonant circuit with a resonant angular frequency $\omega_L \simeq$??.?krad/s.

2.2.3 Frequency Response with the Resistor Voltage Difference as Circuit Output

Considering the voltage difference across the resistor as the circuit output, we will have instead

$$H_R(\omega) = \frac{j\omega RC}{1 - \omega^2 LC + j\omega RC}.$$

Using the definition of Q and ω_0, and after some algebra, $H_R(\omega)$ becomes

$$H_R(\omega) = \frac{j\omega\frac{\omega_0}{Q}}{\omega_0^2 - \omega^2 + j\omega\frac{\omega_0}{Q}}\,. \tag{2.3}$$

Computing the magnitude and phase of $H_R(\omega)$, we obtain

$$
\begin{aligned}
|H_R(\omega)| &= \frac{\frac{\omega_0}{Q}\omega}{\sqrt{(\omega_0^2-\omega^2)^2+\left(\omega\frac{\omega_0}{Q}\right)^2}} \\
\arg\left[H_R(\omega)\right] &= \arctan\left(Q\,\frac{\omega_0^2-\omega^2}{\omega\omega_0}\right)
\end{aligned}
$$

The magnitude has maximum for

$$\omega_R^2 = \omega_0^2,$$

and the maximum is

$$|H_R(\omega_R)| = 1\,.$$

Far from the resonance ω_R, the approximate behavior of $|H_R(\omega)|$ is

$$
\begin{aligned}
\omega \ll \omega_R \quad &\Rightarrow \quad |H_R(\omega)| \simeq \frac{1}{Q}\,\frac{\omega}{\omega_0} \\
\omega \gg \omega_R \quad &\Rightarrow \quad |H_R(\omega)| \simeq \frac{\omega_0}{\omega}
\end{aligned}
$$

Figure 2.4 shows the magnitude and phase of $H_R(\omega)$. In this case the circuit is a first order band pass filter.

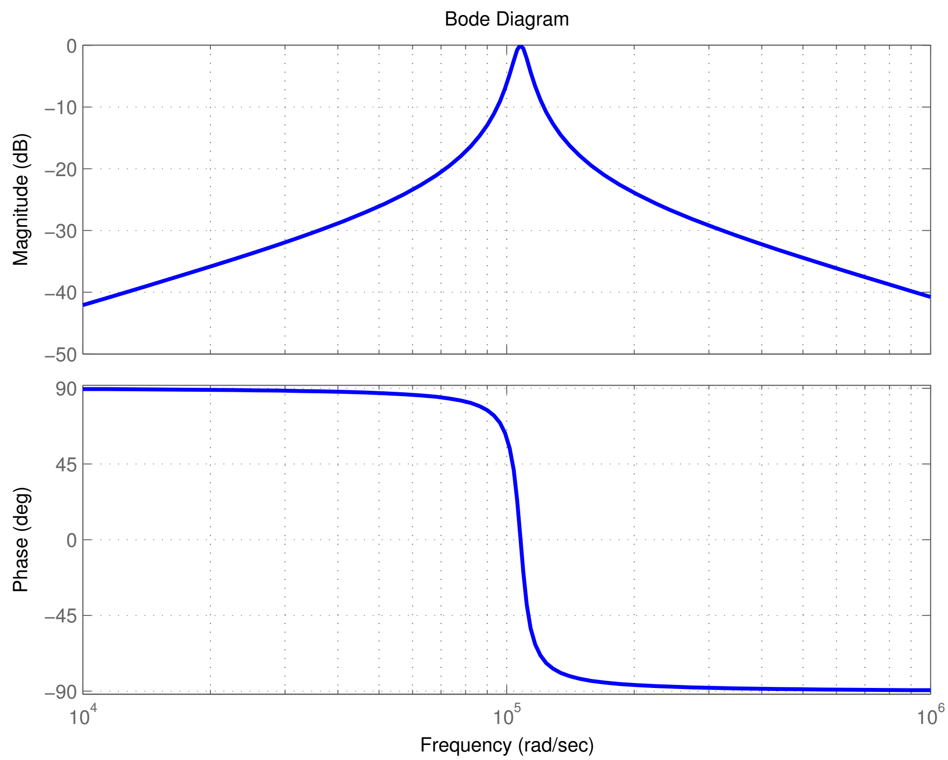


Figure 2.4: Transfer function $H_R(\omega)$ of the LCR series resonant circuit with resonant angular frequency $\omega_R \simeq 10.8$krad/s.

2.2.4 Transient Response

The equation that describes the LCR series circuit response in the time domain is

$$v_i = Ri + L\frac{di}{dt} + \frac{1}{C}\int_0^t i(t')dt' \,, \tag{2.4}$$

where $i(t)$ is the current flowing through the circuit and $v_i(t)$ is the input voltage.

Supposing that

$$v_i(t) = \begin{cases} v_0, & t > 0 \\ 0, & t \leq 0 \end{cases} \,,$$

and differentiating both side of eq. 2.4, we obtain the linear differential equation

$$R\,\frac{di}{dt} + L\,\frac{d^2 i}{dt^2} + \frac{1}{C}\,i = 0, \qquad t > 0$$

or, considering the definition of ω_0, and Q,

$$\frac{d^2 i}{dt^2} + \frac{\omega_0}{Q}\,\frac{di}{dt} + \omega_0^2\,i = 0.$$

The solutions of the characteristic polynomial equation associated with the differential equation are

$$\lambda_{1,2} = -\frac{1}{2}\frac{\omega_0}{Q} \pm \omega_0\sqrt{\frac{1}{2Q^2} - 1}.$$

As usual, we will have three different solutions depending on the discriminant value

$$\Delta = \frac{1}{2Q^2} - 1\ .$$

Under-damped Case: discriminant less than zero $(Q > 1/\sqrt{2})$

In this case we have two complex conjugate roots and the differential equation solution is the typical exponential ring down

$$i(t) = i_0 e^{-\frac{\omega_0}{2Q}t}\sin\left(\omega_C t + \varphi_0\right), \qquad \omega_C^2 = \omega_0\left(1 - \frac{1}{2Q^2}\right)\ .$$

Critically Damped Case: Discriminant equal to zero$(Q = 1/\sqrt{2})$

In this case we have a critically damped current and no oscillation

$$i(t) = i_0 e^{-\frac{\omega_0}{2Q}t}$$

Over-damped Case: Discriminant greater than zero $(Q < 1/\sqrt{2})$

This is the case of two coincident solutions . We will have indeed, an exponential decay (no oscillations)

$$i(t) = i_0 e^{-\frac{\omega_0}{2Q}t}\left(Ae^{-\omega_C t} + Be^{+\omega_C t}\right), \qquad \omega_C^2 = \omega_0^2\left(1 - \frac{1}{2Q^2}\right),$$

Voltages across each single element can be easily computed considering the relation between $v(t)$ and $i(t)$.

Let's just write the voltage across the capacitor for the under-damped case. Considering that the integration operation in this case changes just the phase and creates an offset, the voltage across the capacitor, neglecting this offset, will be

$$v_C(t) = v_0 e^{-\frac{\omega_0}{2Q}t}\sin\left(\omega_C t + \psi\right).$$

2.3 The Tank Circuit or LCR Parallel Circuit.

Figure 2.5 shows the so called *LCR parallel resonant circuit* or *tank circuit*, where the source depicted with an arrow inside a circle is an ideal current source. The resistor of resistance r accounts for inductor resistance. Let's study the frequency and the transient response using the Thévenin representation shown in figure 2.5.

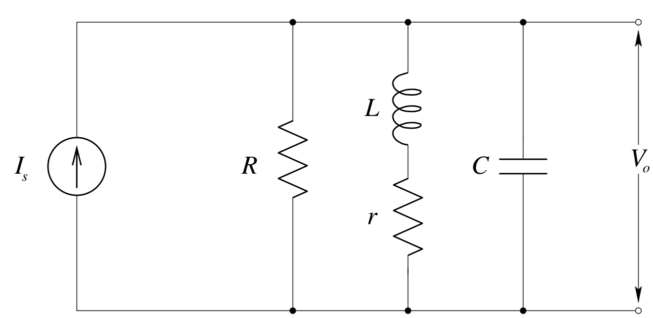


Figure 2.5: The tank circuit.

2.3.1 LCR Circuit Frequency Response

Using Thévenin theorem for the current source and R, the LCR parallel circuit considering the equivalent circuit as shown in figure 2.5 where the current source and the resistor R have been replaced with the Thévenin circuit.

Considering that the current I of the current source can be written as

$$\begin{aligned} I &= \frac{V_i}{R}, \\ I &= Y\,V_o = \left(\frac{1}{R} + \frac{1}{r + j\omega L} + j\omega C\right) V_o, \end{aligned}$$

we have

$$\frac{V_i}{R} = \left(\frac{1}{R} + \frac{1}{r + j\omega L} + j\omega C\right) V_o \tag{2.5}$$

Defining

$$\frac{1}{r^*(\omega)} + \frac{1}{j\omega L^*(\omega)} = \frac{1}{r + j\omega L}\ , \tag{2.6}$$

and

$$R^* = R \,||\, r^*,$$

eq. 2.5 becomes

$$\frac{V_i}{R} = \left(\frac{1}{R^*} + \frac{1}{j\omega L^*} + j\omega C\right) V_o$$

After some algebra, we will have

$$\frac{V_o}{V_i} = \frac{j\omega L^*}{R^* - \omega^2 C L^* R^* + j\omega L^*}\ . \tag{2.7}$$

Generalizing the definition of ω_0, and Q

$$\omega_0^* = \frac{1}{\sqrt{L^*(\omega)C}}, \qquad Q^* = R^*(\omega)\sqrt{\frac{C}{L^*(\omega)}}\ ,$$

and substituting in eq. 2.7 we finally obtain

$$H(\omega) = \frac{j\omega\omega_0^*/Q^*}{(\omega_0^*)^2 - \omega^2 + j\omega\omega_0^*/Q^*}$$

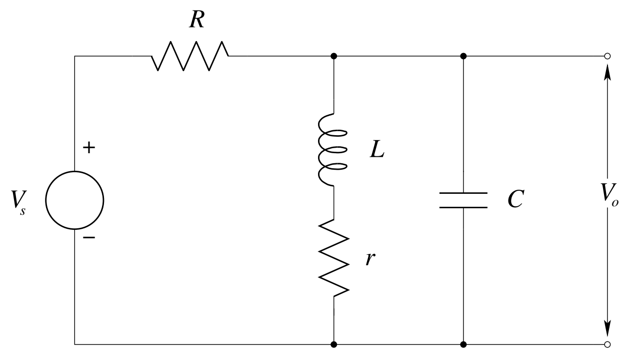


Figure 2.6: The tank circuit with the current source and the resistance R replaced with the Thévenin equivalent circuit.

Let's find the implicitly defined functions r^*, L^*. Using the term containing the inductance L in eq. 2.6, we obtain

$$\frac{1}{r + j\omega L} = \frac{1}{r\left[1 + \left(\frac{\omega L}{r}\right)^2\right]} + \frac{1}{j\omega L\left[1 + \left(\frac{r}{\omega L}\right)^2\right]}.$$

and finally

$$r^*(\omega) = r\left[1 + \left(\frac{\omega L}{r}\right)^2\right], \qquad L^*(\omega) = L\left[1 + \left(\frac{r}{\omega L}\right)^2\right]$$

2.3.2 Transfer Function

From the solution of the LCR parallel circuit we have

$$\begin{aligned} |H(\omega)| &= \frac{\frac{\omega\omega_0}{Q^*}}{\sqrt{\left(\omega_0^2 - \omega^2\right)^2 + \left(\frac{\omega\omega_0}{Q^*}\right)^2}} \\ \arg(H(\omega)) &= \arctan\left\{Q^*\frac{\omega_0^2 - \omega^2}{\omega\omega_0}\right\}, \end{aligned}$$

whose bode plots are shown in figure 2.7.

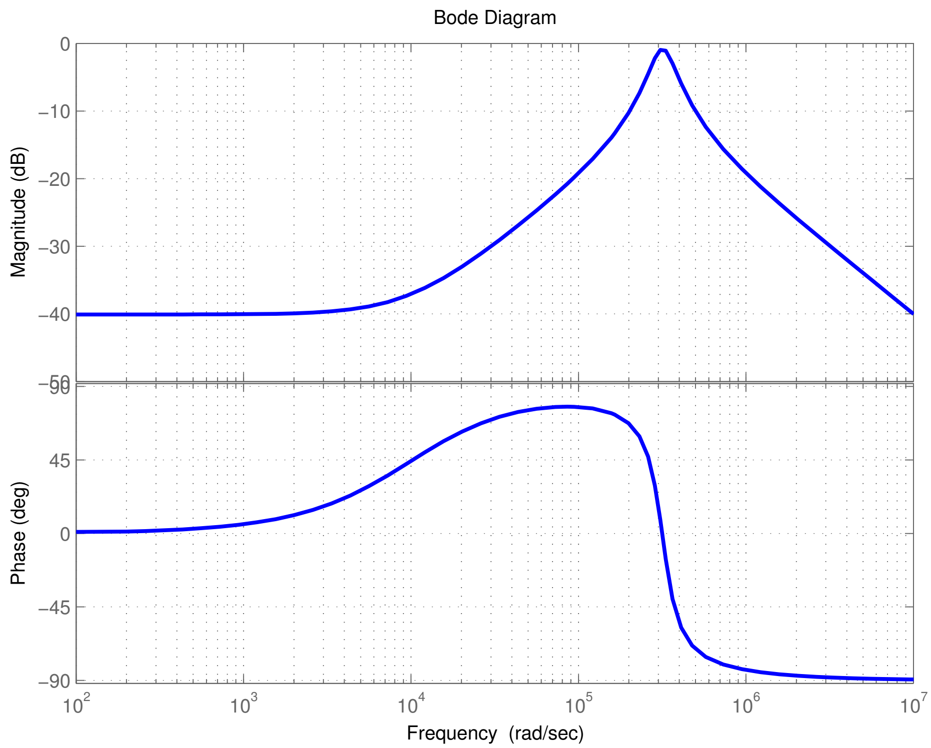


Figure 2.7: Typical bode plot of a LCR parallel circuit with resonant angular frequency near the acoustic band. As expected , if r is not negligible the magnitude doesn't go to zero for $\omega \to 0$.

2.3.3 Simplest Case

It is worthwhile to notice that if $r = 0$ we will have much simpler expressions, i.e.

$$\omega_0 = \frac{1}{\sqrt{LC}}, \qquad Q = R\sqrt{\frac{C}{L}}.$$

and

$$H(\omega) = \frac{j\omega\omega_0/Q}{\omega_0^2 - \omega^2 + j\omega\omega_0/Q}$$

The magnitude and the phase will be

$$\begin{aligned}
|H(\omega)| &= \frac{\frac{\omega\omega_0}{Q}}{\sqrt{(\omega_0^2-\omega^2)^2+\left(\frac{\omega\omega_0}{Q}\right)^2}} \\
\arg(H(\omega)) &= \arctan\left\{Q\frac{\omega_0^2-\omega^2}{\omega\omega_0}\right\},
\end{aligned}$$

2.3.4 High Frequency Approximation

For high frequency $\omega \gg 1$, we have

$$r^*(\omega) \simeq r\left(\omega\frac{L}{r}\right)^2, \qquad \Rightarrow \qquad L^* \simeq L$$

and ω_0 becomes

$$\omega_0 \simeq \frac{1}{\sqrt{LC}}.$$

Evaluating the several defined quantities at ω_0, we will have

$$\begin{aligned}
r^*(\omega_0) &\simeq \frac{L}{rC}, \\
R^*(\omega_0) &\simeq \frac{LR}{RCr+L} \\
Q^*(\omega_0) &\simeq \frac{LR}{RCr+L}\sqrt{\frac{C}{L}}
\end{aligned}$$

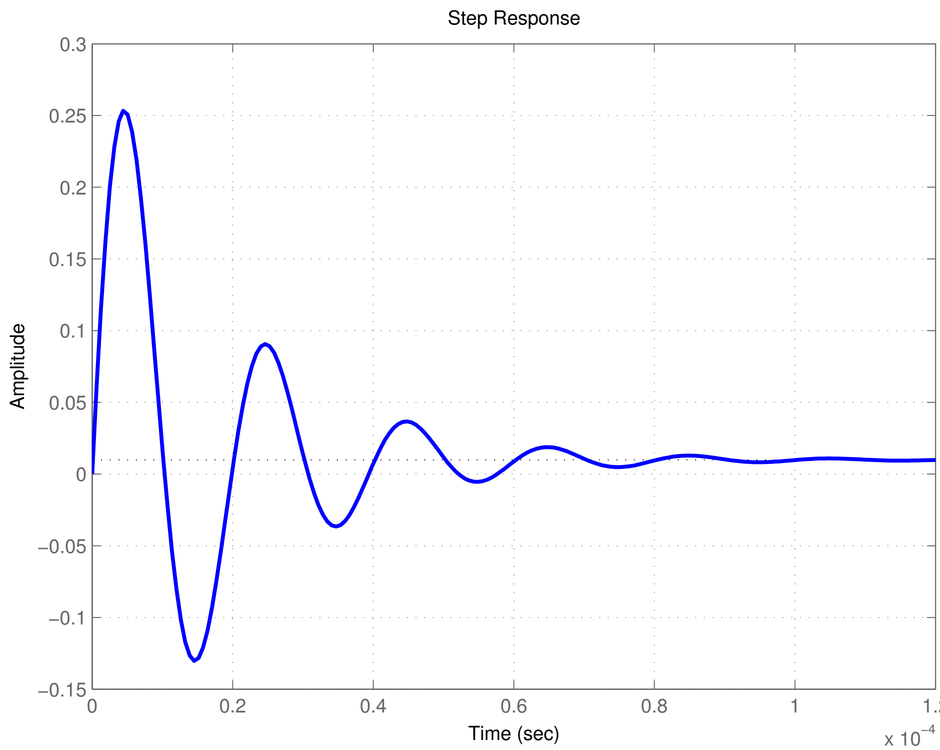


Figure 2.8: Typical step response of a LCR parallel circuit near the acoustic band.

2.3.5 LCR Parallel Circuit Transient Response

Let's briefly analyze the response to a step of the LCR parallel circuit for the under-damped case.

If we define the following quantity

$$\gamma = \frac{1}{2Q},$$

called damping coefficient, and if $0 < \gamma < 1$, then we will have at the circuit output

$$v(t) = v_0 \frac{2\gamma}{\gamma - 1} e^{-\omega_0 \gamma t} \cos\left(\sqrt{1-\gamma^2}\, \omega_0 t + \varphi_0\right) + v_1\,.$$

The voltage output $v(t)$ is a damped sinusoid with angular frequency $\sqrt{1-\gamma^2}\,\omega_0$ and time constant $\tau = 1/\omega_0\gamma$. The DC offset $v_1$depends on the inductor resistance r.

Figure 2.8, a typical step response of the LCR circuit shows a ring-down with a DC offset.

2.4 Laboratory Experiment

Real inductors have not negligible resistance. To build a LCR series circuit with a highest quality factor it is indeed necessary to minimize the resistance of the circuit by mounting in series the inductor and the capacitor only. Typical effective resistance of the inductors used in the laboratory is about 10Ω to 80Ω at resonance .

Because of the internal resistance of the function generator (the best scenario gives $\sim 50\Omega$) is then comparable at some frequencies to LCR load, we will expect that the approximation of ideal generator will be no longer valid.

Moreover, harmonic distortion of the function generator will be quite evident in the LCR series circuit because of the dependence of the load on the frequency.

An estimation of a ring-down time constant τ can be obtained as follows. From the ring-down equation we have that after a time $t = \tau$ the envelope maximum amplitude is reduced by a factor 1/3 ($e \simeq 1/2.718$). This means that we can easily estimate τ by just measuring the time needed to reduce the amplitude down to about $1/3$ of its initial value. A cruder way is to count how many periods n^* the amplitude takes to decrease to 1/3 of its initial value. Then the estimation will be

$$\tau \simeq Tn^* = \frac{n^*}{\nu_0} \, ,$$

where T, and ν are respectively the period and the frequency of the oscillation. Considering that $Q = \pi\nu_0\tau$ then

$$Q \simeq \pi n^* \, .$$

2.4.1 Pre-laboratory Exercises

It is suggested to read the appendix about the electromagentic noise to complete the pre-lab problems and the laboratory procedure.

1. Determine the capacitance C of a LCR series circuit necessary to have a resonant frequency $\nu_C = 20$kHz if $L = 10$mH, and $R = 10\Omega$. Then, calculate Q, τ, ν_0, $(\omega = 2\pi\nu)$ of the circuit.

2. Find the LCR series input impedance Z_i and plot its magnitude in a logarithmic scale. Determine at what frequency is the minimum of $|Z_i|$.

3. Supposing that the internal resistance of the function generator is $R_s = 50\Omega$, and using the previous values for L, C, and R, calculate the circuit input voltage attenuation at the frequency of $|Z_i|$ minimum and at twice that frequency.

4. Determine the capacitance C of a tank circuit necessary to have a resonant frequency $\nu_C = 20$kHz if $L = 10$mH, $R = 10$kΩ, and $r = 10\Omega$. Use the high frequency approximation. Then, calculate Q, τ, ν_0, of the circuit.

5. Estimate the time constant τ of the ring-down in figure 2.8. Supposing that $R = 10$kΩ, estimate r from figure 2.7.

6. Calculate the maximum frequency of the EM field isolated by a Faraday cage with a dimension $d = 10$mm.

2.4.2 Procedure

1. Build a LCR series circuit with a resonant frequency of around 20kHz, using inductance, capacitance, and resistance values calculated in the pre-lab problems. Then, do the following steps:

   (a) Verify the circuit transfer function $H_C(\nu)$ and in particular for frequencies $\nu \ll \nu_C$ and $\nu \gg \nu_C$

   (b) Explain why the input voltage V_i changes in amplitude if we change frequency.

   (c) Considering the harmonic distortion of the function generator, explain why the frequency spectrum of the input signal changes quite drastically when we approach the resonance ν_C.

   (d) Find the resonant frequency ν_C knowing the expected magnitude and phase values, and compare with the theoretical value.

   (e) Estimate the quality factor Q of the circuit from the transfer function measurements and compare it with the theoretical value.

2. Build a LCR parallel circuit with a resonant frequency around 20kHz, using inductance, capacitance, and resistance values calculated in the pre-lab problems. Then, do the following steps:

   (a) Verify the circuit transfer function $H(\nu)$, and in particular for frequencies $\nu \ll \nu_0$ and $\nu \gg \nu_0$.

   (b) Find the resonant frequency ν_0 knowing the approximate expected magnitude and phase, and compare with the theoretical values. Estimate the quality factor Q of the circuit and compare it with the theoretical value.

   (c) Estimate the quality factor Q of the circuit using the step response.

3. Check the effect of the Faraday cage (a metallic coffee can) using 10x probe connected to the oscilloscope. Add a 1m long wire to increase the antenna effect.
   Note the differences when the antenna is approached to the fluorescent lights, and when you touch the antenna.
   Keeping the cage in the same position, explain what you observe and coarsely estimate the amplitude and frequency content of the picked-up signal in the following conditions:

   (a) Antenna outside the cage,

   (b) Antenna inside the cage,

   (c) Antenna inside the cage with ground probe connected to the cage.

Chapter 3

Diodes and Transistors

3.1 Introduction

In this chapter we will analyze two new electronic devices, the semiconductor diode and the bipolar junction transistor (BJT). For a better understanding of their behavior and characteristics, we will also introduce some basic applications.

Unfortunately, there will be no time to study the quite complex physics of semiconductors, and especially the conduction mechanism, which substantially differs from that of metals. The interested student should look for a course and books on solid state physics.

It is important to notice that to quickly grab how the BJT device works, it is fundamental to acquire a clear understanding of the semiconductor diode's behavior.

3.2 The Semiconductor Junction (Diode)

The *semiconductor junction* or *semiconductor diode* is a device which shows non-linear behavior due to its peculiar conduction mechanism.

In fact, if I_D and V_D are the current and the voltage difference across the junction, we will have

$$I_D(V_D) = I_s(e^{\frac{-qV_D}{\eta k_B T}} - 1), \tag{3.1}$$

where I_0 is the reverse saturation current, $k_B = 1.3807 \cdot 10^{-23}$J/K, the Boltzmann constant, T the absolute temperature , $q = -1.60219 \cdot 10^{-19}$C, the

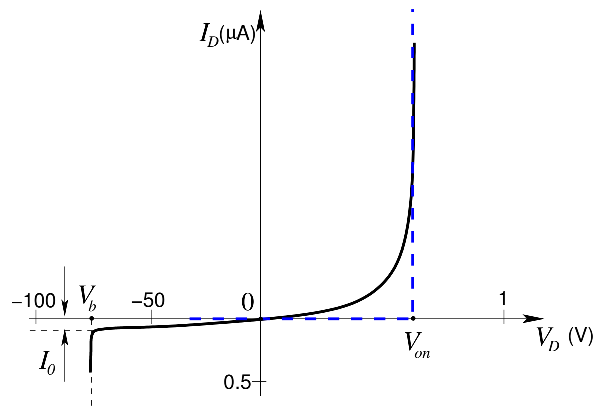


Figure 3.1: Diode characteristic (continuous curve), simplified diode characteristic (dashed curve). Note the different scales in first and third quadrant of the diode characteristic plot.

electron charge, and η a dimensionless parameter which depends on the diode type. Considering that the ambient temperature is $T \simeq 300$K, we will have $k_B T \simeq 4.14 \cdot 10^{-21} J \simeq 0.026 eV$. For silicon diodes the reverse saturation current I_s is of the order of few tenths of nano-amperes.

Instead of following Ohm's law, the semiconductor junction follows an exponential law (the diode I-V Characteristic). Deviations from this law are negligible depending on the current magnitude and the diode characteristics.

Figure 3.1 shows standard symbols for a semiconductor diode and the I-V characteristic. The break-down voltage V_b reported in the same figure is the reverse voltage which essentially short circuits the junction (typically between -100V and -50V). This behavior is not accounted in equation (3.1), and is generated by the so called avalanche multiplication mechanism and the Zener mechanism[1].

[1]The thermally generated carriers accelerated by the electric field have enough energy to disrupt the electrons bond of the crystal atoms producing new carriers (electron-holes pairs). The new and accelerated pairs generate new carriers producing an avalanche of carriers, and indeed a break-down current.

A sufficient strong electric field can also disrupt electrons bonds creating an electron-hole reverse current. This effect is called Zener Breakdown mechanism.

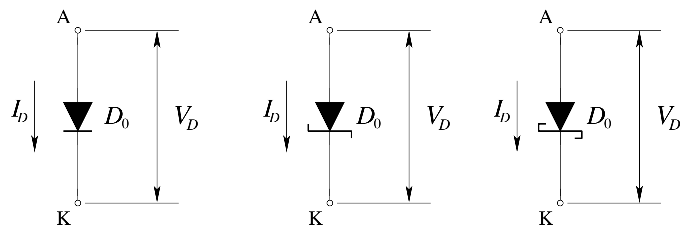


Figure 3.2: diode standard symbols. Starting from left, diode symbol , Zener diode symbol, and Schottky diode symbol. Diode terminals A, and K are respectively called anode and cathode.

A simplified model of the junction diode is that of a perfect switch, i.e.

$$I_D(V) = \begin{cases} \infty & V \geq V_{on} \\ 0 & V < V_{on} \end{cases} ,$$

where V_{on} is the diode *turn-on voltage* or *cut-in voltage*, which depends on the junction type and on the current magnitude. For current up to $I_D \sim 100$mA, silicon diodes have $V_{on} \simeq 0.6$V, and germanium diodes have $V_{on} \simeq 0.3$V .

For voltages greater than V_{on}, the diode is a short circuit (current is not limited by the diode) and is said to be *forward biased*. For smaller values it is an open circuit (current across the diode is zero) and is *reverse biased*.

3.2.1 Zener Diodes

Zener diodes are particular semiconductor diodes with adequate power dissipation to operate in the break-down voltage region. They have a well defined V_b, with values ranging from about few volts to several hundreds volts. Zener diode symbol is shown in figure 3.9. Approximating the characteristics with a piecewise linear relationship, we have

$$I_D(V) = \begin{cases} -\infty & V < V_b \\ 0 & 0 \leq V < V_{on} \\ +\infty & V \geq V_{on} \end{cases} ,$$

Often, the break-down curve is virtually vertical so that the previous approximation of the reverse biased region is quite good.

3.2.2 Schottky Diodes

A junction made of a semiconductor and a metal can behave like a semiconductor diode[2]. For example, Lightly doped silicon and aluminum can form a semiconductor junction. Such kind of devices, called *Schottky barrier diodes* (or simply *Schottky diodes*), still follow the diodes characteristics (3.1) with usually a lower turn-on voltage V_{on} and a larger in magnitude reverse saturation current I_s. The symbol for Schottky diode device is shown in figure 3.9.

3.3 Diode Dynamic Impedance

For linear devices the current is proportional to the applied voltage and for a given frequency the impedance (V/I) is constant. With non-linear circuits this is not true anymore, but we can generalize the impedance concept introducing the dynamic impedance

$$R_d = \frac{dV}{dI}$$

Let's apply this definition to the diode. Starting from the I-V characteristic equation and neglecting the reverse saturation current, after some algebra we obtain

$$V_D = \eta \frac{k_B T}{q} \ln \frac{I_D}{I_0} \,.$$

Taking the derivative on both sides we obtain

$$R_d = \eta \frac{k_B T}{q} \frac{1}{I_D}$$

As we can see, the dynamic impedance of the diode depends on the current I_D.

Considering a silicon diode with a typical value of $\eta = 2$, we will have

$$R_d(I_D) \simeq \frac{5.2 \cdot 10^{-4}}{I_D} \Omega, \qquad I_D = 1\text{mA} \quad \Rightarrow R_d \simeq 0.52\Omega \,.$$

For small variations of the current around 1mA, we can assume that the impedance of a forward biased diode with $\eta = 2$ is $\sim 0.5\Omega$ per milliampere. The dynamic impedance concept will be quite useful for studying the bipolar junction transistor.

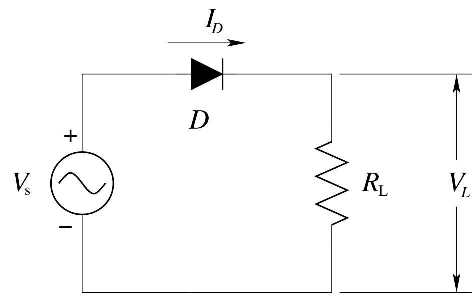


Figure 3.3: Half-wave rectifier circuit.

3.4 Practical Circuits

To better understand the behavior of a semiconductor junction, let's analyze a few typical applications of semiconductor diodes. Some other applications in connection to other components will be studied in the following chapters.

3.4.1 Rectifiers, AC to DC Conversion

The purpose of a rectifier circuit is to convert alternating current into a unidirectional current. This can be achieved using semiconductor diodes. The typical alternating current to direct current converter is a rectifier connected to an active low pass filter with a so called regulator circuit, which smoothes the rectifier output and minimizes ripples. The simplest regulator is a capacitor placed in parallel with the rectifier output. Regulators can be easily found in literature (see [1]).

3.4.1.1 Half-Wave Rectifier

The simplest rectifier circuit is the so called half-wave rectifier shown in figure 3.3.

Using the diode ideal characteristic, it is quite straightforward to predict the voltage difference across the the resistor R_L. In fact, when the sinusoidal signal is positive, it will forward bias the diode and we will have a voltage drop across the resistor $V_L = RI$. For the negative half cycle, because the diode is reverse biased V_L must be zero.

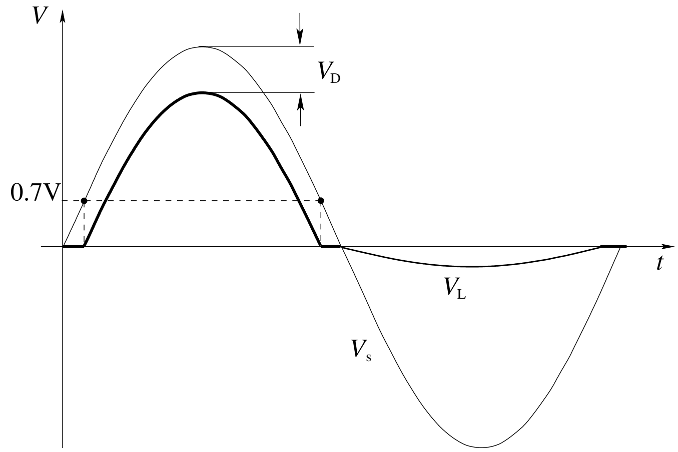


Figure 3.4: Voltage difference across the load connected to the half-wave rectifier output.

Considering the diode threshold voltage V_0, and the diode resistance R_f during the positive half cycle we will have

$$V_L = \frac{R_L}{R_f + R_L}(V_s - V_0),$$

and if

$$R_L \gg R_f \quad \Rightarrow \quad V_L \simeq (V_s - V_0).$$

During the negative half cycle we will have

$$V_L = \frac{R_L}{R_r + R_L} V_s,$$

and if

$$R_L \ll R_r \quad \Rightarrow \quad V_L \simeq \frac{R_L}{R_r} V_s \simeq 0.$$

The main disadvantage of this circuit is the very poor efficiency (less than 50% of current is rectified). In fact, instead of rectifying the entire signal the circuit chops the negative half cycle out (see figure 3.4).

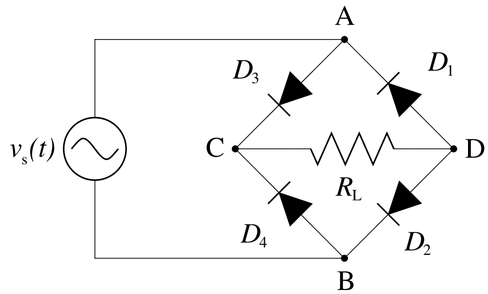


Figure 3.5: Full-wave rectifier bridge circuit or simply bridge rectifier.

3.4.1.2 Full-Wave Rectifier Bridge

The Full-Wave rectifier bridge (see figure 3.5), a more efficient way of rectifying an AC current, uses four arranged diodes in the so called bridge configuration. To understand the circuit "logic", let's consider the two possible states of the nodes A and B shown in figure 3.5.

- When the node A is positive (B negative) the diodes D_2, and D_3 are forward biased (i.e. the diodes are a "short circuit") and D_1, and $D_4$are reverse biased (i.e. the diodes are an "open circuit"). The current flows through the resistor R_L and the node C is positive.
- When the node A is negative (B positive), the diodes D_1, and D_4 are forward biased (short circuit) and D_2, and D_3 are reverse biased. The current flows through the resistor R_L and the node C is still positive.

Using the full-wave rectifier we will indeed have the negative half cycle rectified as shown in figure3.6.

3.4.2 Voltage Limiter (Diode Clamp)

Diodes can be used to limit the voltage applied to an input as shown in figure 3.7. Let's consider the diode D_1connected to V_{max}. If V_i exceeds $V_{max} + V_{on}$ the diode is not reverse biased anymore and starts conducting, i.e the circuit limits the input voltage V_i to $V_{max} + V_{on}$. Analogously, D_2 limits the minimum input voltage V_i to $V_{min} + V_o$. The resistor is necessary to limit the current flowing through the diodes. In fact, without the resistor

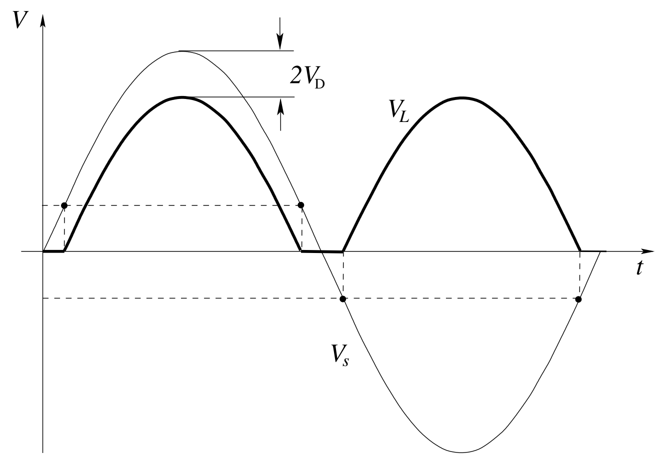


Figure 3.6: Voltage difference across the load connected to the full-wave rectifier output

if we exceed one of the voltage limits an excessive current can destroy the forward biased diode junction. The worst scenario is when the broken diode becomes an open circuit and then the device to protect becomes completely unprotected.

3.5 The Bipolar Junction Transistor (BJT)

The *bipolar junction transistor* is essentially a device formed by two semiconductor junctions which share one semiconductor layer (see figure 3.8).

The common layer is called the *base* and the two others are the *collector* and *emitter*. We will have then the *emitter-base* and the *collector-base* junctions.

There are two types of BJT: the *npn* and the *pnp transistor*. In the pnp transistor the collector and the emitter are p-type and the base is n-type. The npn transistor has a p-type base , and n-type collector and emitter. Standard symbols for both types are shown in figure 3.9.

Because the two junctions have two possible states (forward or reverse biased), the BJT can have four possible operating modes as shown in the following table

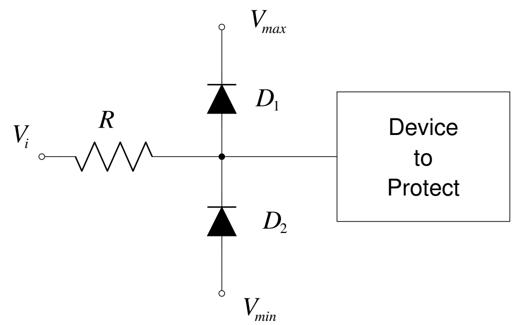


Figure 3.7: Diode clamps circuit.

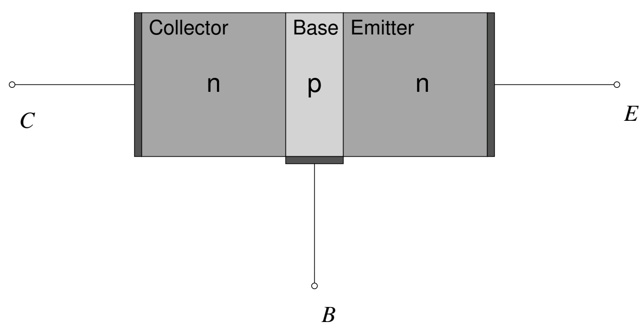


Figure 3.8: Qualitative physical model of a npn junction.

Operating Mode	Bias Emitter-Base	Bias Collector-Base
Forward-Active	Forward	Reverse
Cutoff	Reverse	Reverse
Saturation	Forward	Forward
Reverse-Active	Reverse	Forward

Forward-Active:

The BJT approximates a current-controlled source of current as explained in section 3.5.2.

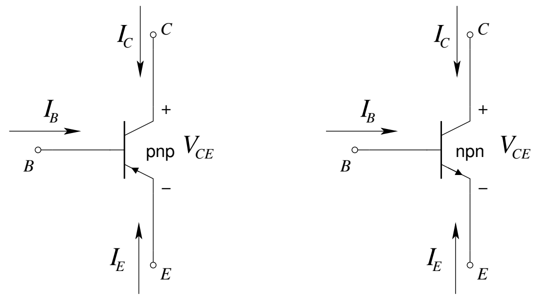


Figure 3.9: Standard circuit symbols for npn and pnp transistors.

Cutoff:

Both junctions are reverse biased. Neglecting the reverse saturation current, no current flows through the junctions. This mode, together with the saturation mode, is used to implement the switch device (see section3.5.5).

Saturation:

Both junctions are forward biased, and the current I_C flows from the collector through the emitter.

Reverse-Active:

The BJT still approximates a current-controlled source of current, but the amplification factor is usually less than that of the forward-active mode.

3.5.1 The Collector Emitter Characteristic

Figure 3.10 shows collector emitter characteristic curves family of a typical npn transistor. Each curve corresponds to a given value of the base current I_B, with the base emitter junction forward biased.

The curves have three regions which are called, the *saturation*, *forward-active*, and *breakdown* regions. The break-down region starts for V_{CE} values larger than those shown in the plots .

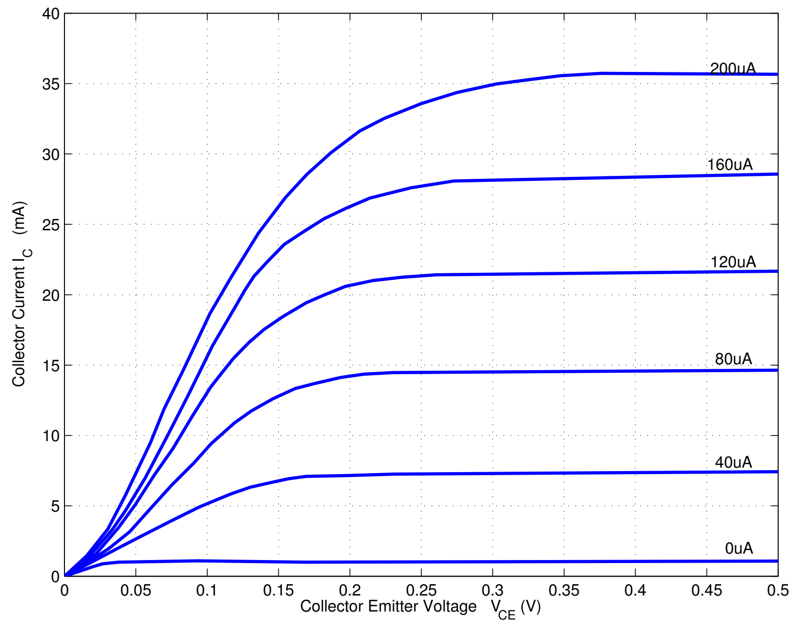


Figure 3.10: Collector Emitter voltage characteristics for the 2N2222 npn transistor. The value above each curve is the corresponding base current I_B.

Saturation Region

The saturation region is where the collector emitter voltage difference V_{CE} slightly changes as a function of the collector current I_C. For the 2N2222 this regions is where V_{CE} is between 0V to about 0.3V.

Forward-Active Region

The collector current I_C slightly changes as a function of the collector emitter voltage V_{CE}. Normally, this region is quite larger than the saturation region. For the 2N2222 it is where V_{CE} is between 0.3V to about 50V.

Break-Down Region

This is the region where the V_{CE} doesn't change and I_C rapidly increases. In this case, the conduction in the junction is produced by the avalanche

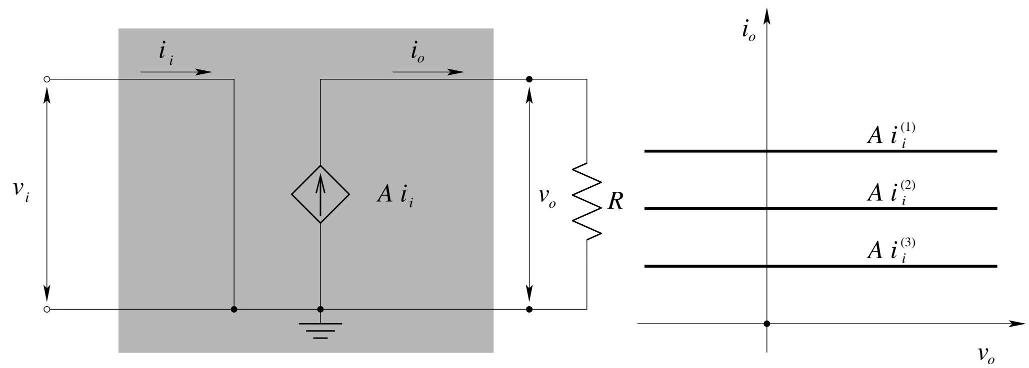


Figure 3.11: Ideal current controlled source (diamond symbol), i.e. the current output i_o is proportional to the current input i_i, and is independent of the load R. In other words, if we change the load R and v_o consequently, i_o stays constant.

mechanism. For the 2N2222 this region starts from $V_{CE} > 60$V.

3.5.2 The BJT as a Current-Controlled Current Source (CCCS)

As stated before, the bipolar junction transistor is a device that approximates a current-controlled source of current CCCS (see figure 3.11). In other words, because its current output i_o is proportional to the current input i_i we can linearly control i_o by changing i_i, i.e.

$$i_o(t) = \beta_F \, i_i(t).$$

if $|\beta_F| > 1$ then the BJT is a current amplifier.

As shown in figure 3.11, once i_i is set i_o must be constant independently of the load R placed at the output. If the voltage across the output $v_o$changes we don't expect to see any changes on i_o. The curve height simply depends on the current input i_i.

This approximation is valid for the so called small signal model and the low frequency model. Non linearities arise for large signals and at high frequency the response cannot be flat.

It is clear from the V_{CE} characteristic that, if we want to use the BJT as CCCS , we have to bias it with a DC voltage to work in the forward-active region.

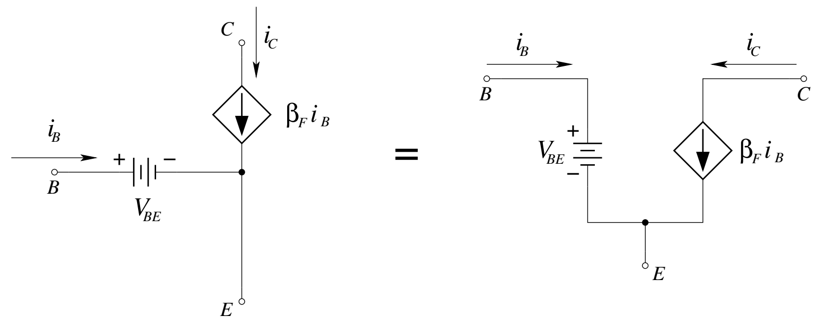


Figure 3.12: Simplified DC model for the bipolar junction transistor working in forward-active mode. The two drawings are just two different arrangement of the same circuit.

3.5.3 BJT Simplified DC Model

The simplified DC model of the BJT for the forward-active mode is shown in figure 3.12 with two different arrangements. The first mimics the topology of the BJT symbol, and the second the topology of the CCCS in figure 3.11. This model is good enough to properly bias the transistor to work as an amplifier.

The current controlled current source represents the V_{CE} characteristic in the forward-active region. The battery in the base emitter circuit represents the voltage across the base-emitter forward biased junction (it could be replaced with a diode). A typical value is $V_{BE} = 0.7$V.

3.5.4 The BJT as an Amplifier

Left circuit of figure 3.13 shows the basic configuration of a BJT as a simple current amplifier. Resistors R_B and R_C are chosen to properly bias and limit the currents across the junctions. The capacitance at the input is necessary to prevent the DC bias from reaching the device connected to the amplifier input. Let's better analyze how to properly bias the transistor junctions.

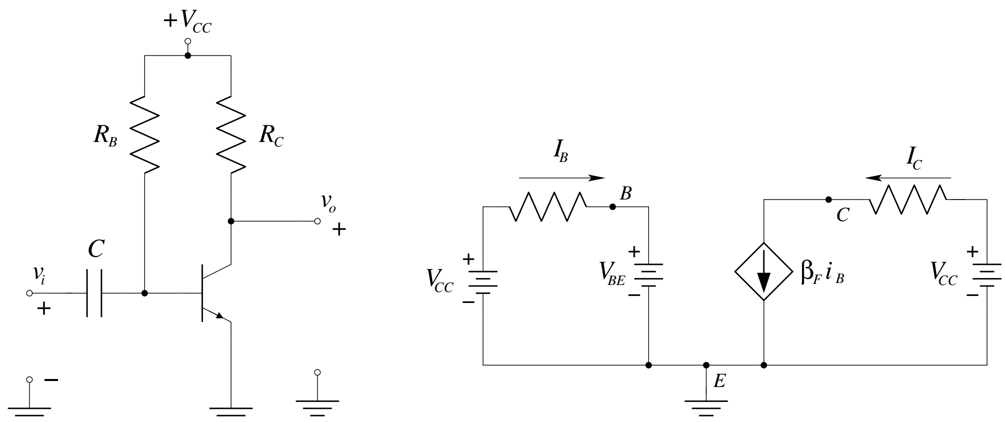


Figure 3.13: The BJT as an AC basic amplifier (left), and same circuit using the forward-active DC model (right).

3.5.4.1 BJT Amplifier Bias

To obtain the largest voltage dynamic range, and considering the V_{CE} characteristic, and neglecting the saturation region, we must have

$$V_{CC} \simeq 2\,V_{CE}\,. \tag{3.2}$$

Plugging this forward-active DC model into the amplifier circuit as shown in figure 3.13, we will have[2]

$$V_{CC} = V_{CE} + R_C I_C,$$

Considering equation3.2 and the previous equation the collector resistor value will be

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{V_{CE}}{\beta_F I_B}.$$

For the base resistor we will have

$$V_{CC} = V_{BE} + R_B I_B,$$

[2]The repeated index is a common convention used to distinguish between the voltage of the transistor's connections and the source voltages applied to the transistor connections. In this case between the collector voltage V_C and the source voltage V_{CC}.

and finally

$$R_B = \frac{2V_{CE} - V_{BE}}{I_B}\,.$$

This circuit is not very useful because the junctions bias and the gain depend on β_F, which is quite often not well know and can easily vary by a factor of two for the same transistor. Moreover, $\beta_F$is quite sensitive to temperature fluctuations. Anyway, this circuit is pedagogically interesting because of it simplicity.

Numerical Example

A typical BJT a transistor has V_{CE} between 1V and 10V. Considering the following parameters

$$\begin{cases} \beta_F &= 100 \\ V_{CE} &= 5\text{V} \\ V_{BE} &= 0.7\text{V} \\ I_B &= 80\mu\text{A} \end{cases} \Rightarrow \begin{cases} R_C &\simeq 625\Omega \\ R_B &\simeq 116.25\text{k}\Omega \\ V_{CC} &\simeq 10\text{V} \end{cases}\,.$$

3.5.4.2 BJT Amplifier Gain, Input and Output Impedance (Low Frequency Model)

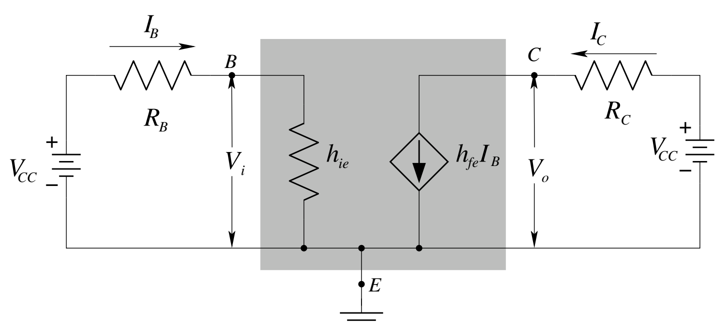


Figure 3.14: BJT basic amplifier using the low frequency model (gray box). The parameters $h_{fe} = \beta_F$and h_{ie} are provided by the manufacturer

Because the emitter-base junction is forward biased the input impedance seen from the points B and E is quite low. This consideration with the fact that the BJT approximates a CCCS is sufficient enough to define a model for the BJT transistor response for the low frequency region. Figure 3.14 shows the model applied to the basic amplifier. The resistance h_{ie} is indeed the dynamic input impedance of the forward biased emitter-base junction.

From figure 3.14 we can easily calculate the amplifier voltage gain, which is

$$|A_v| = \frac{R_C I_C}{h_{fe} I_B} = h_{fe} \frac{R_C}{h_{ie}} \qquad (\beta_F = h_{fe})$$

Considering that the ideal current source is an open circuit and the ideal voltage source is a short circuit, we will have

$$R_i \simeq R_B || \, h_{ie}, \qquad R_o \simeq R_C \, .$$

Thermal fluctuations can substantially change the response of the BJT. A way to avoid such kind of behavior is to add a feedback network. Essentially, a feedback network samples the output and sends it back to the input with negative sign minimizing the output fluctuations. For example, if the amplifier gain increases because of a temperature increase, the feedback signal will increase as well reducing the input signal by the amount necessary to keep the gain constant. Feedback networks can create instabilities due phase delays in the loop (the feedback signal can change sign). It is indeed necessary to satisfy stability criterion to avoid oscillations. A detailed explanation of feedback theory can be found in [2] and [3].

3.5.5 BJT as Switch

Figure 3.15 shows a npn BJT configured as a switch. In this case, the function of the two resistors R_B and R_C are just to limit the current flowing through the transistor junctions.

The input voltage v_i control the output state of the switch. For sake of simplicity let's neglect the reverse currents components to study the circuit.

- If $v_i = 0$, The emitter-base junction is reverse biased and no current flows through the circuit. This implies that $v_o \simeq V_{CC}$ and (BJT in cutoff state).

- If $v_i = V$ and supposing that this voltage forward bias both junctions we will have $v_o \simeq 0$ (BJT in saturation).

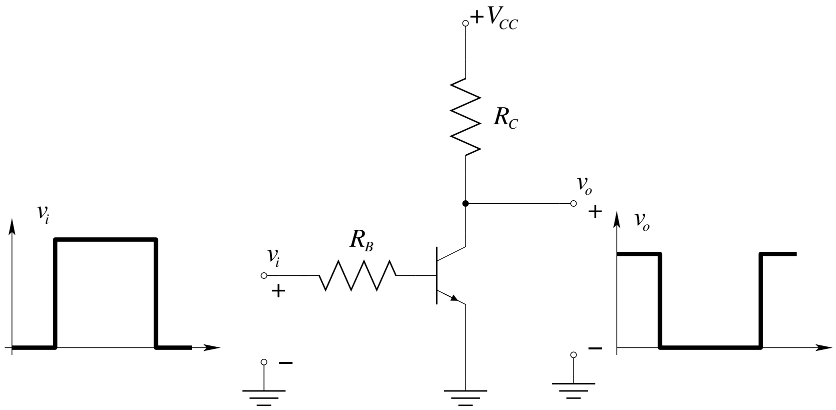


Figure 3.15: BJT as a switch

Let's consider now the BJT reverse currents.

- If $v_s = 0$, we will have $i_C = I_{CO}$ and $v_o = V_{CC} - I_{CO}R_C$. Because $I_{CO} \sim 1$nA $I_{CO}R_C$ is negligible and $v_0 = V_{CC}$.
- If $v_i = V$, then v_0 is essentially the voltage drop $V_{BE}$of the forward biased base-emitter junction $v_o = 0.7$V.

3.5.6 BJT as Diode

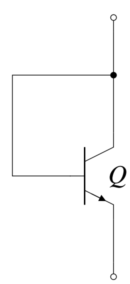


Figure 3.16: BJT as diode.

Figure 3.16 shows the typical configuration used to make a BJT working as simple diode. The emitter-base junction acts as a simple semiconductor diode. Short circuiting the collector-base ensures that the collector-base junction is always reverse biased.

3.5.7 Current Mirror

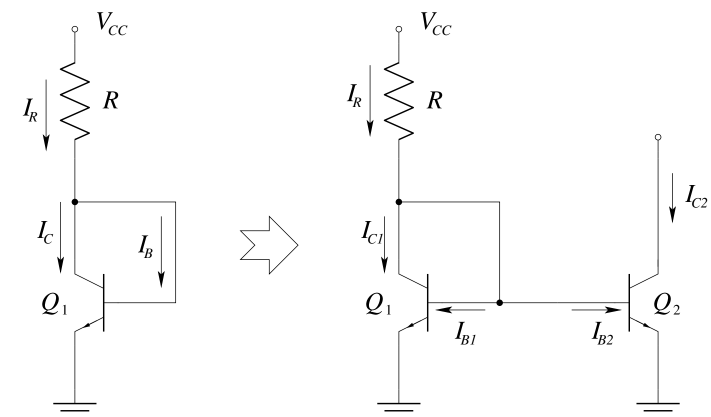


Figure 3.17: BJT as diode.

Let's consider the left circuit shown in figure 3.17 where V_{CC}forward bias the emitter-base junction. From the KVL obtain

$$I_R = \frac{V_{CC} - V_{BE}}{R}.$$

If V_{CC} and R are kept constant ($V_{BE} = 0.7$, typically) then I_R is constant as well. Applying the KCL to node we obtain

$$I_R = I_C + I_B$$

and considering that

$$I_c = \beta I_B$$

we will finally have

$$I_R = \left(1 + \frac{1}{\beta}\right) I_C. \quad \Rightarrow I_C \simeq I_R.$$

The collector current I_C is indeed constant if $V_{CC}$and R are kept constant.

Let's now consider the circuit on the right-hand side of figure 3.17. Because of the KVL we will have

$$V_{BE1} = V_{BE2}$$

Supposing that the two transistors Q_1 and Q_2 are perfectly identical and because they have the same V_{BE}we must have

$$I_{C1} = I_{C2}.$$

We will have indeed that the output I_{C2} will work as a constant current source.

Let's analyze the stability of the circuit for a change on the transistor parameter β. From the KVL and KCL we have

$$\begin{aligned} I_R &= \frac{V_{CC} - V_{BE}}{R} \\ I_R &= I_C + 2I_B \end{aligned}$$

After some simple algebra and considering that $I_C = \beta I_B$we will have

$$I_C = \frac{\beta}{\beta + 1} \frac{V_{CC} - V_{BE}}{R}$$

Studying the fluctuation of the transistor we will have

$$\frac{\Delta I_C}{I_C} \simeq 2\frac{\Delta\beta}{\beta^2} .$$

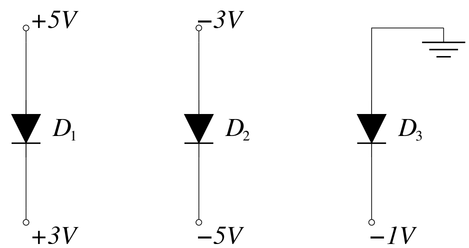
In other words, the stability of this current source due to the fluctuations of the transistor properties are expected to be remarkably good. In fact, if we suppose to have $\beta = 100$ and change of 100% in β then

$$\left\{ \begin{array}{rcl} \beta &=& 100 \\ \Delta\beta &=& 100 \end{array} \right. \qquad \Rightarrow \frac{\Delta I_C}{I_C} \simeq 0.02$$

For their simplicity, current mirror are extensively used in ICs design where a constant current source is needed.

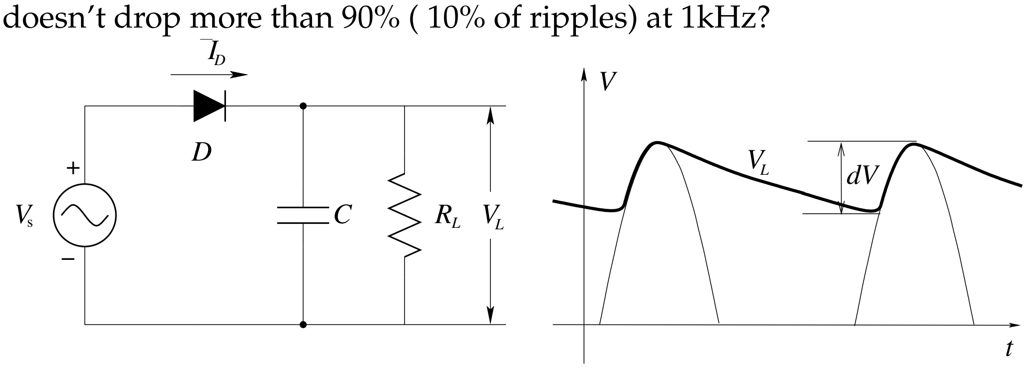
3.6 Pre-Laboratory Problems

1. Considering the following figure, state which cases have the diode conducting



2. Calculate the resistance R needed to limit the current flowing through a diode to 10mA with a voltage source of $V_s = 5$V.

3. Adding a Capacitor C in parallel to the the half-wave rectifier load R_L we low-pass filter the rectifier. If the load $R_L = 1\text{k}\Omega$, what must be the value of the capacitor C (within 10%) so the voltage output doesn't drop more than 90% (10% of ripples) at 1kHz?



(Hint: consider that the capacitor is just discharging through the load R_L).

4. Estimate the β of the npn transistor 2N2222 in figure 3.10.

5. Supposing that we want a maximum current of 1mA going through the base, and the maximum applied input voltage is 5V, determine the value of R_B for the BJT switch circuit.

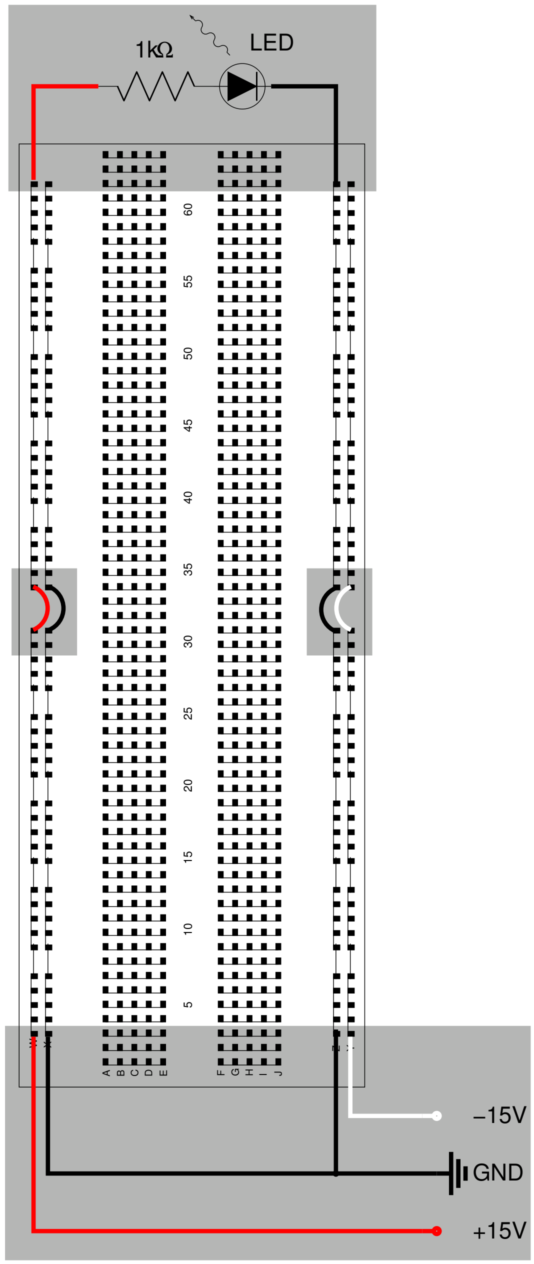


Figure 3.18: Electronic circuit breadboard contacts topology and suggested connections. Power supplies voltage distribution and LED connections are highlighted with gray boxes. Whenever possible black jacket wires should be used to connect components to ground (GND) , red jacket wires for $+15V$ and white jacket wires for $-15V$. This pragmatism helps to understand and debug the circuit.

3.7 Procedure

Remember to consult the components data-sheets to properly connect diodes and transistors leads.

It is good practice to check the power supply connections before turning generators or sources on.

Use a LED (light emitting diode) to indicate the status of power supplies. Connect the LED to the 15V power supply, and limit the current to about 10-20mA.

It is recommended to cable power supplies and LED as shown in figure 3.18. The figure also shows how the contacts are electrically connected inside the breadboard.

To simplify circuits understanding and debugging, use black jacket wires to connect components to ground, red jacket wires for $+15V$ and white jacket wires for $-15V$.

1. Using the half-wave rectifier circuit and the oscilloscope in the $X-Y$ mode, plot the volt-ampere characteristic of a silicon, and a germanium diode. Use channel 1 to measure the voltage drop across the diode the ADD and channel 2 INVERTING features to obtain the voltage across the resistor.
   Verify the exponential response of the diodes and determine their turn on voltage V_{on}. Supposing that the sinusoidal signal amplitude is 5V, choose R to limit the current to a maximum of 10mA.

2. With a 1kHz sinusoidal signal verify the response of the previously built half-wave rectifier comparing the rectifier output with the voltage source signal. Then connect a capacitor in the proper way to obtain ripples of about 10% of the maximum output voltage.

3. Build a BJT switch working with the TTL logic levels $ON \Rightarrow\sim 5$V and $OFF \Rightarrow\sim 0$V.
   Check the status of the two junctions measuring the voltage drop across them for the cut-off and the saturation mode.
   Connecting two silicon diodes to the BJT switch input in a proper way implement a NOR GATE, i.e. a circuit with two inputs A and B and one output C which fulfills the following true table:

A	B	$A\,OR\,B$	$C = \overline{A\,OR\,B}$
OFF	OFF	OFF	ON
OFF	ON	ON	OFF
ON	OFF	ON	OFF
ON	ON	ON	OFF

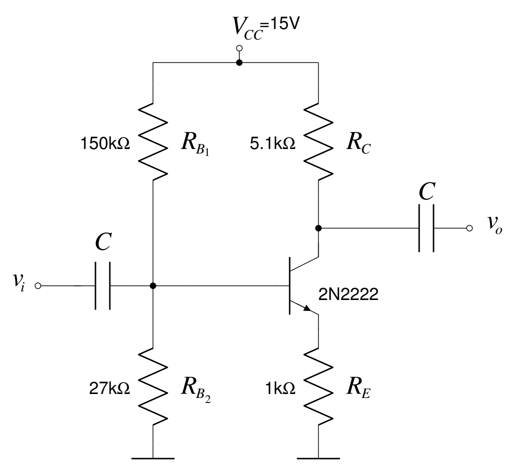
Hint: one lead of each diode should be connected to the switch input. Explain why the diodes are needed.

4. Build the Simple BJT amplifier explained in section 3.5.4 using a 2N2222 transistor, and do the following steps

   (a) Check the DC bias V_{CE} and V_{BE} of the two BJT junctions .

   (b) Measure the transfer function, and find the two cutoff frequencies where the amplitude is -3dB down from the plateau.

5. Optional: Build the following common emitter amplifier circuit (the circuit is explained in the appendix)



and do the following steps

   (a) Check the DC bias V_{CE} and V_{BE} of the two junctions .

   (b) Measure the transfer function, and find the two cutoff frequencies where the amplitude is -3dB down from the plateau.

(c) Verify that the transfer function plateau has a gain $|G| \simeq R_C/R_E$.

Bibliography

[1] ??Find a reference to Regulators??

[2] Microelectronics, Jacob Millman & Arvin Grabel, McGraw-Hill Electrical Engineering Series.

[3] The art of Electronics Second Edition, Paul Horowitz & Winfield Hill, Cambridge University Press

Chapter 4

The Operational Amplifier

4.1 Introduction

Operational amplifiers are one of the most extensively used analog integrated circuits especially because of their ability to approximate reasonably well the ideal behavior. For this reason real operational amplifiers can be quite often modeled as ideal. This simplicity of usage and mostly the versatility this device, which hides a large internal complexity [1], make the operational amplifier suitable for many different applications.

The ideal operational amplifier concept introduced in the first section, will look after a first reading quite awkward. Anyway, everything will be clearer when it is analyzed in conjunction with the called feedback network which links the output of the amplifier inputs.

Subsequent sections are mainly dedicated to the explanation of some basic circuits. Finally, section 4.4 introduces more realistic model of operational amplifier together with some of the peculiar behavior of this electronic device.

4.2 The Ideal Operational Amplifier

The ideal operational amplifier (Op-Amp) is a linear amplifier with two differential inputs v_+, v_- and one output v_o (see figure 4.1) and with the

[1] A modern operational amplifier made of a cascade of stages, each one designed mainly to match the ideal characteristics, can have around 50 components both active and passive. See the Analog Devices Web site, for example.

following characteristics:

- $v_0 = A_v(v_+ - v_-), \qquad A_v > 0$, (linearity)
- input resistance $R_i \to \infty$,
- output resistance $R_o \to 0$,
- voltage gain $A_v \to \infty$,
- frequency response constant for any frequency.

Aside the welcome property of linearity and infinite frequency response, the need of all the other characteristics can be justified as follows. Infinite input resistance R_i means essentially that the Op-Amp inputs do not produce perturbations to any circuit to which they are connected to. Zero output resistance R_o perfectly isolates the Op-Amp from any perturbation. Infinite input impedance and zero output impedance implies also no dissipation of energy. The condition of infinite voltage gain A_v is necessary if we want a device able to deliver any gain, once a network which connects the output to the input is added to the Op-Amp. In general, this kind of network is called *feedback network*.

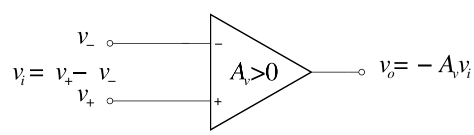


Figure 4.1: Op-Amp symbol.

4.2.1 Fundamental Equation for the Ideal Op-Amp (the Golden Rule)

The consequence of the following conditions

- $A_v \to \infty$,
- $v_o < \infty$ if $v_i = v_+ - v_- < \infty$,

implies

$$v_+ - v_- = 0, \qquad \text{(at all times)} \tag{4.1}$$

Equation 4.1 will be called the *Op-Amp golden rule* and is fundamental for the solution of any circuit involving Op-Amps. We will see in the next sections the importance of this equation once a feedback network is connected to the Op-Amp.

4.2.2 Op-Amp Input Output "Logic"

It is worthwhile here to notice the behavior of Op-Amp output as function of the two inputs. From the definition of Op-Amp we have that a signal sent to the negative input V_- is amplified and changed in sign. A signal sent to the positive input V_+ is just amplified. Two signals sent each to one input are indeed subtracted and amplified.

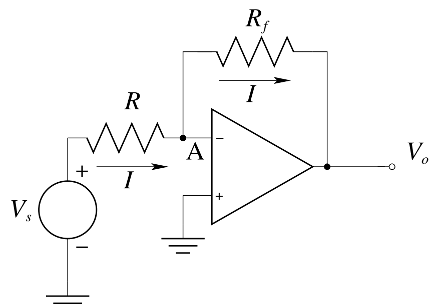


Figure 4.2: Op-Amp with a feedback network.

4.2.3 Op-Amp with a Feedback Network

Let's consider the circuit in figure 4.2, where a feedback resistance R_f is connected to the negative input. The current through the resistors R and R_f is the same because the ideal Op-Amp input does not drive any current ($R_i = \infty$). Furthermore, since $V_i = V_+ - V_- = 0$ and with the use Ohm's law and the KVL, it follows that

$$I = \frac{V_i}{R} = -\frac{V_o}{R_f}. \tag{4.2}$$

The output voltage V_o and voltage gain A will be

$$V_o = AV_i, \qquad A = -\frac{R_f}{R}.$$

The gain of the Op-Amp depends just on the resistances ratio R_f and R.

4.2.4 The Virtual Ground

Let's re-analyze the circuit in figure 4.2. Because of the golden rule $V_i = V_+ - V_- = 0$, and the negative input is grounded, the node **A** must always be at zero voltage. This is equivalent to having **A** virtually grounded. The adjective virtual is necessary, otherwise we could not have $R_i = \infty$. In other words, the virtual ground happens to be because the Op-Amp does its best to keep $V_i = 0$.

4.3 Commonly Used Op-Amp Circuits

In the study of the several common Op-Amp configurations, we will use the approximation of an ideal circuit. A more realistic model is often necessary to understand some behaviors of real circuits. For an initial design, and where the the ideal Op-Amp characteristics are well approximated, the ideal model is quite often sufficient.

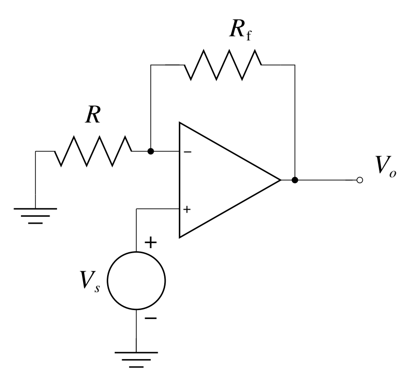


Figure 4.3: Non-inverting configurations of the Op-Amp.

4.3.1 Non-Inverting Amplifier

Let's consider the non-inverting configuration of the Op-Amp in figure 4.3. Because of $V_i = 0$, we will have

$$V_s - V_- = V_s - RI = 0.$$

Considering that the output voltage V_o is

$$V_o = (R_f + R)I,$$

we can use the expression of I to obtain

$$V_s = \frac{R}{R + R_f} V_o.$$

The output voltage V_o and voltage gain A will be

$$V_o = AV_i, \qquad A = 1 + \frac{R_f}{R}.$$

Considering that in this configuration V_s is directly connected to $V_+$and V_- is not a virtual ground, the input impedance of the amplifier is $R_i + R$, where R_i is the real input impedance of the Op-Amp.

4.3.2 Inverting Amplifier

This circuit has been already discussed in section 4.2.3. For completeness, the solution and some comments are here reported

$$V_o = AV_i, \qquad A = -\frac{R_f}{R}.$$

It is worthwhile to notice that because $V_- = 0$, the circuit input impedance is just R. Having values of R typically of few $k\Omega$, the inverting configuration doesn't preserve the high impedance characteristic of an Op-Amp. A connection of the circuit input to a network can potentially create appreciable perturbations.

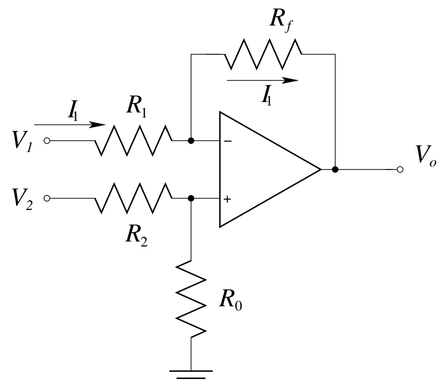


Figure 4.4: Differential input configuration of the Op-Amp.

4.3.3 Differential Input Stage

Let's now solve the differential input circuit of the Op-Amp in figure 4.4.

Writing the voltage drop across $R_1$and R_f, we obtain the linear system

$$\begin{aligned} V_- - V_1 &= R_1 I, \\ V_o - V_+ &= R_f I. \end{aligned}$$

Solving the system with respect to V_o, we get

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_- - \frac{R_f}{R_1} V_1.$$

Using the voltage divider equation to obtain $V_+$and because $V_+ - V_- = 0$, we have

$$V_- = V_+ = \frac{R_0}{R_2 + R_0} V_2,$$

and finally, we get

$$V_o = \frac{R_1 + R_f}{R_1} \frac{R_0}{R_2 + R_0} V_2 - \frac{R_f}{R_1} V_1.$$

A way to to obtain the same voltage gain for V_2 and V_1 is to impose $R_0 = R_f$ and $R_1 = R_2 = R$. The output voltage becomes

$$V_o = A(V_2 - V_1), \qquad A = \frac{R_f}{R}.$$

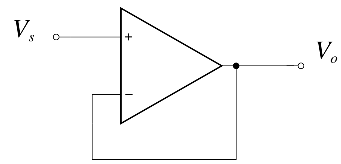


Figure 4.5: Voltage follower or unity gain buffer.

This differential configuration is not very convenient because it does not preserve the high input impedance of the Op-Amp. In fact , considering that the Op-Amp input impedance is very high, we have that the resistance seen from V_1 is $R_2 + R_0$. Usually, the sum of those resistors is at least one order of magnitude smaller than the Op-Amp input impedance.

Moreover, if we need to build a variable gain differential amplifier, we will need to change more than one resistor value. Matching the resistances values can become an issue when thermal drifts become important. More practical and stable configurations called Instrumentation amplifiers are available "off the shelf".

4.3.4 Voltage Follower (Unity Gain "Buffer")

The circuit sketched in figure 4.5 is called voltage follower or unity gain buffer. The feedback line with no load gives

$$V_o = V_+.$$

Moreover, because of the condition $V_i = 0$ we will have

$$V_- = V_+,$$

which implies

$$V_o = V_i.$$

The output follows the input voltage with unitary gain.

Considering that the high impedance input and the low impedance output values of Op-Amps are close to the state of the art in the electronic design[2], the voltage follower can be used as an isolation stage (buffer) between two circuits.

4.3.5 Integrator Amplifier

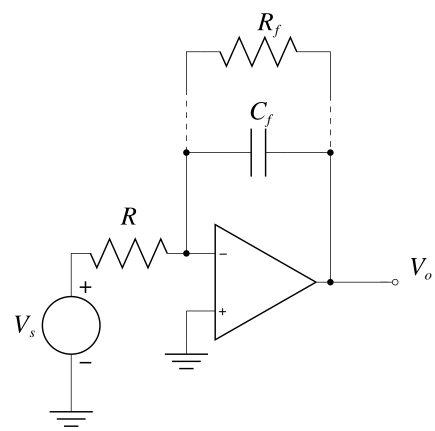


Figure 4.6: Active integration stage using an Op-Amp.

Let's consider the circuit in figure 4.6 without the resistance R_f. The voltage drop v_o across the capacitor C_f is

$$v_o(t) = -\frac{1}{C_f}\int_{-\infty}^{t} i(\tau)d\tau \tag{4.3}$$

and the current flowing through the resistance R is

$$i(t) = \frac{v_i(t)}{R}.$$

Placing the expression of $i(t)$ obtained from the previous equation into eq.(4.3), we will obtain

[2]Devices expressly made to work as input unity gain buffer, and output unity gain buffer are also available. Analog Devices SSM2141 and SSM2142 are complementary buffers devices which can drive long delay lines for example.

$$v_o(t) = -\frac{1}{\tau}\int_{-\infty}^{t} v_{in}(t')dt', \qquad \tau = RC_f.$$

Real Op-Amps or signals connected to the input have often (always) a DC offset. This offset is indeed integrated and after a given time will saturate the amplifier output. This saturation is essentially a manifestation of the instability of the circuit at low frequency. Moreover, the initial charge of the capacitor is undefined, making the initial output state unpredictable.

A common way to avoid these problems is to introduce the resistance R_f in parallel with the capacitor C_f which reduces the amplifier DC gain. An intuitive way to understand the effect of this feedback resistance is that it does not allow the capacitor to be charged ad libitum. The choice of the R_f is not so trivial if we want to preserve the characteristic of good integrator. Using the simple phasor analysis it easy to proof that the good integrator condition is $\omega \gg 1/C_f R_f$.

If the DC current must be integrated, we can place a switch in parallel with the capacitor to be opened when the integration is started. In this way we will have the capacitor state completely defined.

4.3.6 Differentiator Amplifier

Let's now consider the circuit in figure 4.7 without the feedback capacitor C_f. Applying a similar analysis to that used in the integrator amplifier we will have

$$\begin{aligned} i(t) &= C\frac{dv_i}{dt}, \\ v_o(t) &= R_f i. \end{aligned}$$

and indeed

$$v_o(t) = \tau\frac{dv_i}{dt}, \qquad \tau = R_f C.$$

This configuration without C_f doesn't work well with real Op-Amps, because of stability problems. In fact, the introduction of the capacitor compromises the internal compensation of the Op-Amp. Placing a capacitor C_f in the feedback network restores the compensation making the

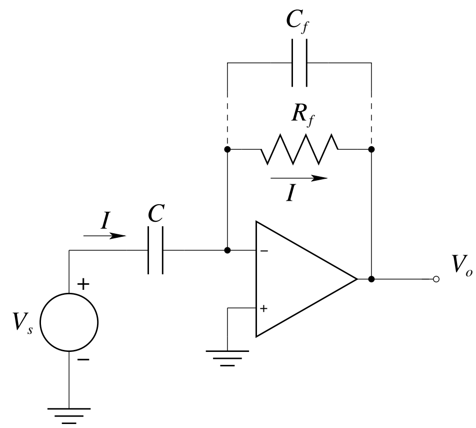


Figure 4.7: Differentiator stage using an Op-Amp.

overall circuit stable. The choice of C_f is not trivial if we want to preserve the circuit differentiator characteristics.

Section 4.4.3 explains in more details the effect of this configuration on the compensation of a real Op-Amp.

4.4 The Real Op-Amp

Lets consider in this section a more realistic model of the Op-Amp by including a finite input impedance R_i, non zero output impedance R_o, finite gain A, bias currents and voltage offsets. Using ideal components, the equivalent circuit of the real Op-Amp is shown in figure 4.8.

4.4.1 Bias Currents and Voltage and Current Offsets

Imbalances inside of the Op-Amp, mainly due to differences in the electronics components, produce undesirable bias currents and a voltage offset at the inputs. Input voltage and current offsets can be modeled by introducing ideal generators as shown in figure 4.8. Current Offset is defined as the difference in the magnitude of the bias currents, i.e.

$$i_{os} = |i_{b+}| - |i_{b-}|$$

A way to characterize the voltage offset is to use the voltage follower configuration (see section 4.3.4) with the input V_i connected to the ground. The voltage offset will be directly the output voltage V_o.

Current input biases can be studied connecting a resistor between the one input and ground and measuring the voltage drop across the resistor.

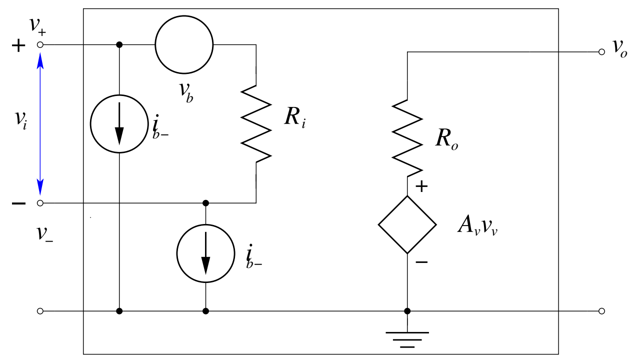


Figure 4.8: Equivalent circuit for an Op-Amp using ideal components. Voltage offsets and current biases are taken into account using ideal voltage and current generators.

4.4.2 Feedback Amplifiers

Let's consider an amplifier with a negative feedback network as show in figure 6.1. Considering that the summation point output is

$$V_i - \beta(\omega)V_o,$$

FeedbackAmp.eps not found!

Figure 4.9: Amplifier with negative feedback

and the amplifier gain is $A(\omega)$, the output voltage must be

$$V_o = A(V_i - \beta V_o),$$

Collecting V_o we will have

$$V_o = \frac{A}{1+\beta A} V_i \, ,$$

and the amplifier response A_{CL} (the so called *closed loop transfer function*) will finally be

$$A_{CL}(\omega) = \frac{A}{1+\beta A}.$$

We can clearly see that if the denominator goes to zero for a given frequency ω^* we are in trouble, $A_{CL}(\omega^*)$ diverges, and the amplifier saturates. The trick to avoid this situation, is to study the following equation

$$A_{OL}(\omega) = -1, \qquad A_{OL} = \beta \, A \, .$$

where A_{OL} is the *feedback amplifier open loop transfer function*. If the phase where the magnitude of A_{OL} is equal to one is different from 180^0plus multiples of 360^0 the denominator never goes to zero and the saturation is avoided. However, this is not enough because we can have just an oscillation with no saturation if the A_{OL} phase is too close to 180^0. The rule of thumb is to have a so called *phase margin* of about 60^0 from -180^0. Finally, we can formulate a criterion for the stability:

$$\text{where } |A_{OL}| = 1 \qquad \Rightarrow 120 > \arg(A_{OL}) > -120$$

Another important result of the theory of feedback amplifier is the following straightforward result

$$\text{if} \quad \beta A \gg 1 \qquad \Rightarrow \qquad A_{CL}(\omega) \simeq \frac{1}{\beta}$$

Where the open loop transfer function $A\beta$ is greater than one the feedback amplifier response does not depend on the response $A(\omega)$ of the amplifier with no feedback.

It is worthwhile to notice that the ideal amplifier has $A \rightarrow \infty$ and the feedback amplifier response becomes $A_{CL} = 1/\beta$ for all angular frequencies. Therefore, the ideal amplifier does not have undesired instabilities, but just those ones that can be introduced by the feedback network.

4.4.2.1 Non-Inverting Configuration

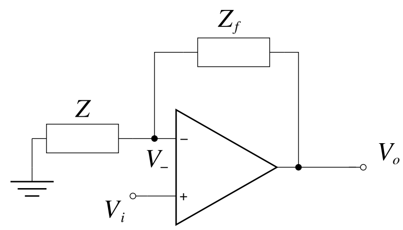


Figure 4.10: Non-inverting configuration Op-Amp with generic impedance.

Considering the Op-Amp Non-Inverting configuration as shown in figure 4.10, and the voltage divider equation we have

$$V_- = \frac{Z}{Z_f + Z} V_o \,, \tag{4.4}$$

and the feedback network transfer function is

$$\beta(\omega) = \frac{V-}{V_0} = \frac{Z}{Z_f + Z} \,.$$

The approximate gain of the feedback amplifier is as expected

$$A_{CL} \simeq \frac{1}{\beta} = 1 + \frac{Z_f}{Z} \,.$$

4.4.2.2 Inverting Configuration

In this case the feedback network transfer function β is

$$\beta = \frac{V_i}{V_0} \,.$$

Considering the inverting configuration stage as shown in figure 4.11, and because of the virtual ground we have

$$\begin{cases} V_i &= ZI \\ -V_o &= Z_f I \end{cases} \quad \Rightarrow \quad \beta(\omega) = -\frac{Z}{Z_f} \,,$$

The gain of the feedback amplifier is simply

$$A_{CL} \simeq \frac{1}{\beta} = -\frac{Z_f}{Z} \,.$$

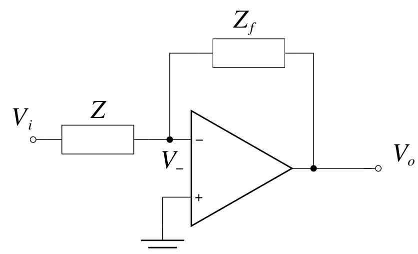


Figure 4.11: Inverting configuration Op-Amp with generic impedance.

4.4.3 Compensated Op-Amp Transfer Function

Practical Op-Amps are often designed to have a frequency response dominated by a single pole, i.e. the transfer function with no feedback is just a simple low-pass filter. In this case, the Op-Amp transfer function with no feedback can be written as

$$A(\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_0}}, \tag{4.5}$$

where A_0 is the DC gain and ω_0 is the angular frequency of the dominant pole (the cut-off angular frequency of the low pass filter). This behavior is obtained by introducing a compensating circuit (quite often a capacitor) in the architecture of the Op-Amp.

Typical values for pole frequencies are between 5Hz and 100Hz. Figure 4.12 shows the differential transfer function of the Op-Amp AD711 with no feedback network.

The reason of this choice comes from the stability requirement that we mentioned in the previous section. In fact, an amplifier with a dominant pole transfer function with dominant pole cannot lose more than 90^0 making quite easy the design of a feedback network. To better understand, let´s study more in details the compensated Op-Amp response with a feedback.

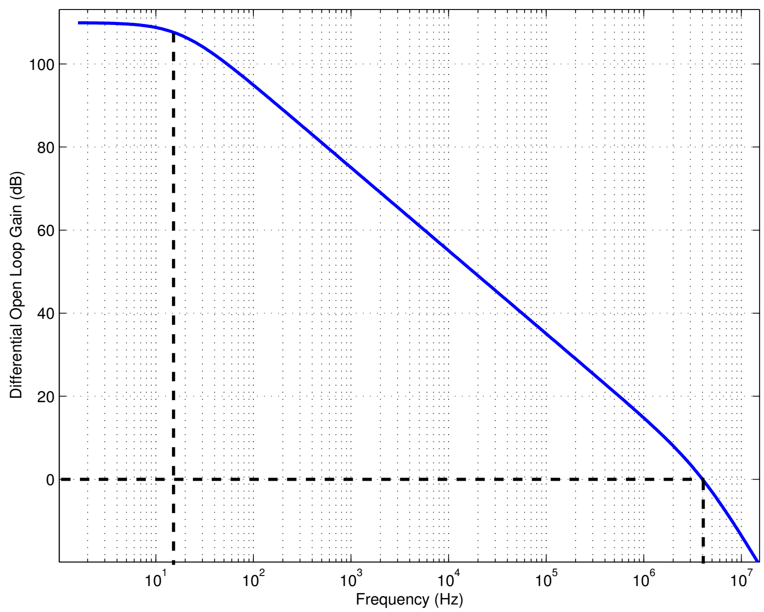


Figure 4.12: Differential gain of the AD711 Op-Amp (cut-off frequency $\nu_0 =$ 18Hz, unity gain frequency $\nu_1 = 4$MHz, and DC gain $a_0 = 110$dB).

4.4.3.1 Compensated Op-Amp Frequency Response with Feedback

Considering the frequency response of a feedback amplifier for the compensated case we will have

$$\begin{aligned} A(\omega) &= \left(\frac{A_0}{1+j\frac{\omega}{\omega_0}}\right) \Bigg/ \left(1+\frac{\beta(\omega)A_0}{1+j\frac{\omega}{\omega_0}}\right) \\ &= \frac{A_0}{1+\beta(\omega)A+j\frac{\omega}{\omega_0}} \\ &= \left(\frac{A_0}{1+A_0\beta(\omega)}\right) \Bigg/ \left(1+j\frac{\omega}{\omega_0(1+\beta(\omega)A_0)}\right) \end{aligned}$$

In the particular case that β is constant and $\beta = \beta_0 \geq 1$, the previous equation becomes

$$A(\omega) = \frac{A_1}{1+j\frac{\omega}{\omega_1}}, \qquad \left\{ \begin{array}{lcl} A_1 &=& \frac{A_0}{1+A_0\beta_0} \\ \omega_1 &=& \omega_0(1+\beta_0 A_0) \end{array} \right.$$

In other words, the feedback Op-Amp response is the same as of the open loop transfer function A_{OL}but with a smaller DC gain (about $1/\beta_0$) and higher cut off angular frequency $\omega_1 \simeq \omega_0\beta_0 A_0$.

4.4.4 The Common Mode Rejection Ratio (CMRR)

We want characterize the rejection of an Op-Amp output as a differential amplifier, of signals sent to both inputs. For an ideal Op-Amp we expect to obtain $V_o = 0$ for all frequencies, i.e. a perfect rejection. To define a convenient parameter which measures the rejection it is necessary to define the following ones, the *common mode gain*

$$A_C(\omega) = \frac{V_o}{V_+ - V_-}, \qquad V_+ = V_- = V_s \sin(\omega t),$$

and the *differential mode gain*

$$A_D(\omega) = \frac{V_o}{V_+ - V_-}, \qquad V_+ = V_s \sin(\omega t), \quad V_- = 0.$$

The *Common Mode Rejection Ratio ($CMRR$)* is defined as the modulus of the ratio of the differential gain A_D over the common mode gain A_C, i.e.

$$CMRR(\omega) = \left| \frac{A_D(\omega)}{A_C(\omega)} \right|$$

Ideally, the $CMRR$ should be infinity for all frequencies.

This parameter can be measured using the Op-Amp differential configuration (see figure 4.4) and measuring A_C and A_D as a function of the frequency. To minimize possible large systematic errors, it is necessary to have the same gain for the to inputs V_1 and V_2. This can be achieved by placing a trimmer in the voltage divider mesh of the differential configuration circuit. Adjusting the trimmer we can minimize V_o for a single frequency and study the $CMRR$ for a given bandwidth.

Figure 4.13shows the $CMRR$ as a function of frequency of a typical Op-Amp. A typical value for $CMRR$ is 90dB.

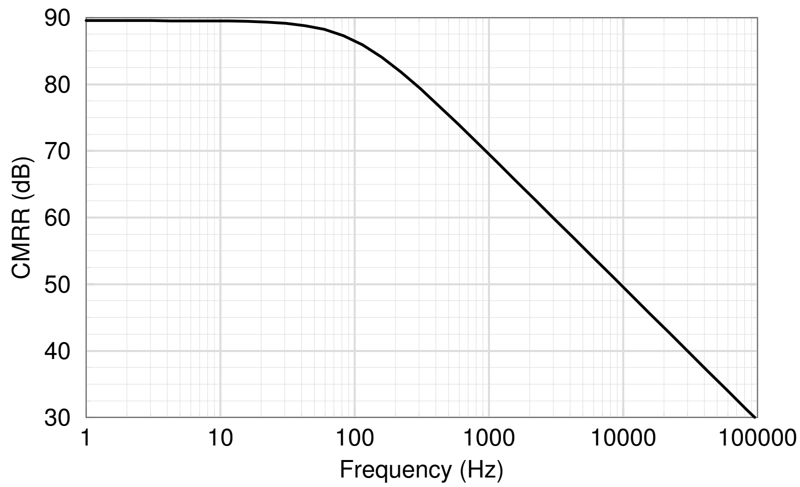


Figure 4.13: $CMRR$ as a function of frequency of a typical Op-Amp.

4.4.5 The Gain Bandwidth Product (GBWP)

The gain bandwidth product is a common way to characterize the gain with respect to the avaliable bandwidth of amplification. It is defined as

$$GBWP = A_0\omega_0.$$

The larger the GBWP the better is the Op-Amp, and the closer the Op-Amp is to the ideal operational amplifier.

4.4.6 The Slew Rate (SR)

The slew rate is defined as the maximum rate of the output voltage v_o per unit time

$$SR = \max\left\{\frac{\Delta v_o(v_i)}{\Delta t}\right\}.$$

This parameter essentially measures the ability of an Op-Amp to follow voltage changes for large voltage inputs.

The slew rate can be easily observed sending a square wave (see figure 4.14) to the Op-Amp input v_i, and looking at the raising and falling slope of the output signal v_o. If the slopes do not change changing the input amplitude, then the Op-Amp is slew rate limited.

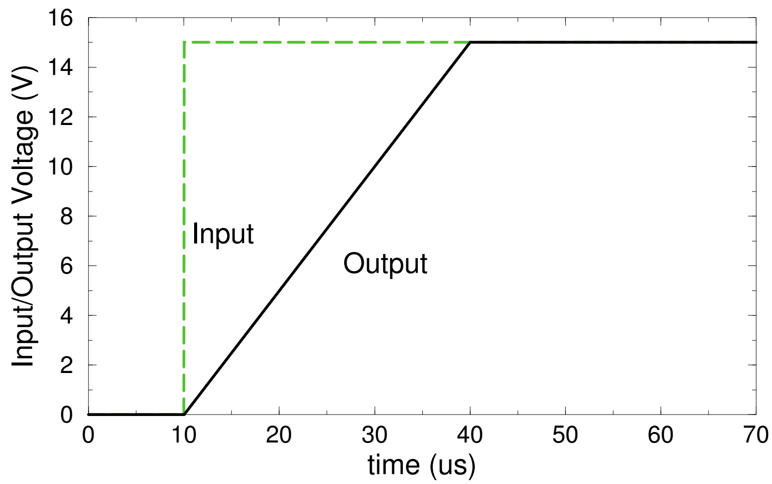


Figure 4.14: Slew rate illustration. Voltage Response v_o of the Op-Amp to a large step input voltage v_i.

A similar procedure can be applied using a low frequency sinusoidal signal as input. In this case if we increase to much the input amplitude, the output will become distorted.

The slew rate is a non-linear effect intrinsic of the architecture of the Op-Amp. In a compensated Op-Amp it is often proportional to the capacitance of the compensating network of the gain stage. Typical slew rate values are of the order of few V/μs.

4.4.7 Ideal versus Real and Practical Considerations

The following table summarizes the main characteristic of an ideal Op-Amp together with those of typical real Op-Amp. In some cases we can found Op-Amps excelling some of the mentioned characteristics, and often being detrimental to others.

Property	Ideal Op-Amp	Typical Op-Amp
Open-Loop DC Gain A_v	∞	$> 10^4$
Open-Loop Bandwidth	∞	$\sim$ 10Hz (dominant pole)
Common Mode Rejection Ratio $CMRR$	∞	$>$ 70dB
Input Resistance R_i	∞	$>$ 10MΩ
Output Resistance R_o	0	$< 500\Omega$
Input Current $\delta I_{\pm}$	0	$< 0.5\mu$A
Input Offset Voltage $\delta V_{\pm}$	0	$<$ 10mV
Input Offset Current δI_i	0	$<$ 200pA

What are the conditions that dictate the range of the feedback impedances R_f? Apart from special cases, the feedback current I should be only a small fraction of the maximum output current I_o, i.e. $I = 1\% I_o$. A typical Op-Amp has a maximum output of 10mA at 10V, i.e.

$$R_f = \frac{V}{I} = \frac{10\text{V}}{10 \cdot 0.1\%\text{mA}} = 100\text{k}\Omega$$

Typical feedback resistors should be in the range of $R_f = 50 - 1\text{M}\Omega$.

Small difference on the differential stage of the Op-Amp produces a DC offset δV at the input, which can produce large DC output if the gain is extremely high. For example, if we have

$$\delta V = 10\text{mV}, \quad G \geq 10^4, \Rightarrow V_o \geq 10V.$$

4.5 Problems Preparatory to the Laboratory

1. Supposing that the open-loop gain of an Op-Amp is a low pass filter with DC gain 144dB and cut-off frequency $f_0 = 10$Hz, sketch in a bode diagram, the magnitude of the frequency response of a non-inverting stage with gain $G = 10$ at 10Hz.

2. Prove that the good integrator condition for the circuit in figure 4.6 is $\omega \gg 1/R_f C_f$. (Hint: calculate the response of the circuit and compare it with the ideal response of the ideal inverting integrator, i.e. $A(\omega) = -1/(j\omega RC)$. Calculate the DC gain of the integrator transfer function.

3. Using an integrator stage with a feedback resistor R_f, and time constant $\tau = RC$, compute the values for τ and R_f needed to integrate a sinusoidal wave with frequency $f > 1$kHz and with 10% of losses in the integration. Choose a value of $R \gg R_s$, where $R_s = 50\Omega$ is the input impedance of the used function generator.

4. Show that the slope of an integrated square wave is the inverse of of the time constant $\tau = RC_f$ of the Integrator shown in figure 4.6. Which characteristics of the square wave are needed to fulfill the requirement to not saturate the integrator output ?

5. Consider a differential stage having the following resistances values: $R_1 = R_2 = 50\text{k}\Omega$, $R_f = R_0 = 100\text{k}\Omega$. Calculate the following quantities

   (a) the two input impedances $Z_1$and Z_2 ,

   (b) the output impedance Z_0,

   (c) Considering that the Op-Amp max output current and voltage are respectively I_{max} =10mA and $V_{max} = 10$V, calculate the smallest load R_{min} it can drive .

6. The output impedance of an Op-Amp is $R_i = 50\Omega$, and its open-loop gain is that shown in figure 4.12. Sketch in an approximate asymptotic Bode plot the Op-Amp magnitude impedance as a function of the frequency.

4.6 Laboratory Procedure

Read carefully the entire procedure before starting the experiment, and note on your log book all the unpredicted behavior you experience in the circuits response.

Consult the data-sheet to properly map the $\mu 741$ and AD711 Op-Amp pin-out.

Op-Amp output high frequency noise can be reduced by adding 100nF capacitors closest as possible to the $\pm 15V$ power supplies input of the Op-Amp.

Before powering your circuit up, cross-check the power supply connections.

It is always a good practice to turn on the power supplies at the same time to avoid potential damages of the Op-Amps.

Using the $\mu 741$ Op-Amp, do the following steps:

- Using a non-inverting configuration with a gain of 100, verify the transfer function of the Op-Amp.
- Using the same previous circuit, estimate the slew rate of the Op-Amp. Redo the same measurement using an AD711 Op-Amp.
- Study the $CMRR$ using a differential configuration. Use a potentiometer to balance the gains at just one frequency and then measure the $CMRR$. Verify that the obtained values are in agreement with the specifications reported in the Op-Amp data-sheet. Mount and tune the null adjustment circuit as specified in the Op-Amp data-sheet.

Build an integration stage using an Op-Amp having a time constant $\tau \sim 100\mu s$. Include a feedback resistor R_f to avoid saturation at the output and do the following steps:

- Measure the impulse response.
- Measure the frequency response.
- Estimate the integrator time constant τ using a square wave.

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[1] The Art of Electronics, Paul Horowitz and Winfield Hill, Cambridge University Press.

[2] Microelectronics Jacob Millman & Arvin Grabel, McGraw-Hill Electrical Engineering Series

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Chapter 5

Basic Op-Amp Applications

5.1 Introduction

In this chapter we will briefly describe some quite useful circuit based on Op-Amp, BJT transistors and diodes.

5.1.1 Inverting Summing Stage

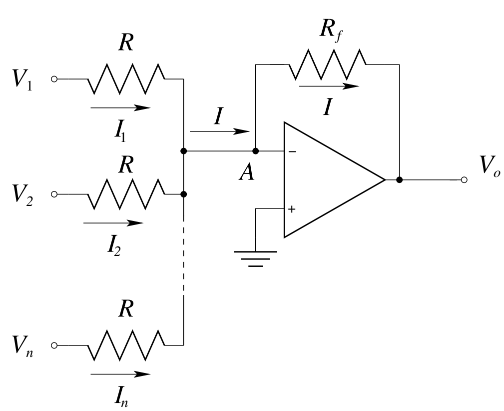


Figure 5.1: Summing stage using an Op-Amp.

Figure 5.1 shows the typical configuration of an inverting summing stage using an Op-Amp. Using the virtual ground rule for node A and

Ohm's law we have

$$I_n = \frac{V_n}{R}, \qquad I = \sum_{n=1}^{N} I_n.$$

Considering that the output voltage V_0 is

$$V_o = -R_f I,$$

we will have

$$V_o = A \sum_{n=1}^{N} V_n, \qquad A = -\frac{R_f}{R}.$$

5.1.2 Basic Instrumentation Amplifier

Instrumentation amplifiers are designed to have the following characteristics: differential input, very high input impedance, very low output impedance, variable gain, and good thermal stability. Because of those characteristics they are suitable to be used as input stages of electronics instruments.

Figure 5.2 shows a configuration of three operational amplifier necessary to build a basic instrumentation amplifier. Some of the problems of the the differential amplifier of figure 4.7 are still present in this circuit, such as how to implement the variable gain, and gain thermal stability. For better architectures see [3].

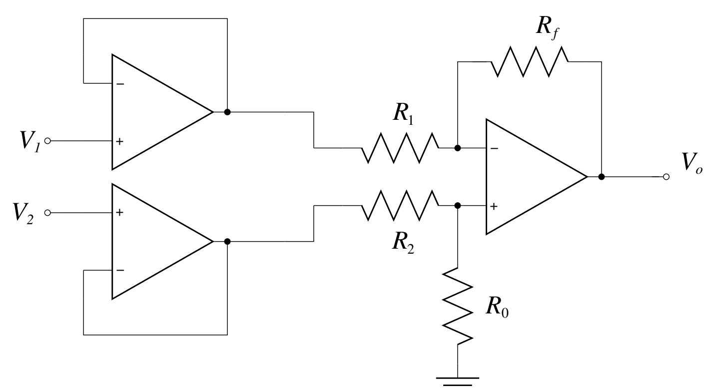


Figure 5.2: Basic instrumentation amplifier circuit.

5.1.3 Voltage to Current Converter (Transconductance Amplifier)

A voltage to current converter is an amplifier that produces a current proportional to the input voltage. The constant of proportionality is usually called *transconductance*. Figure 5.3 shows a Transconductance Op-Amp, which is nothing but a non inverting Op-Amp scheme.

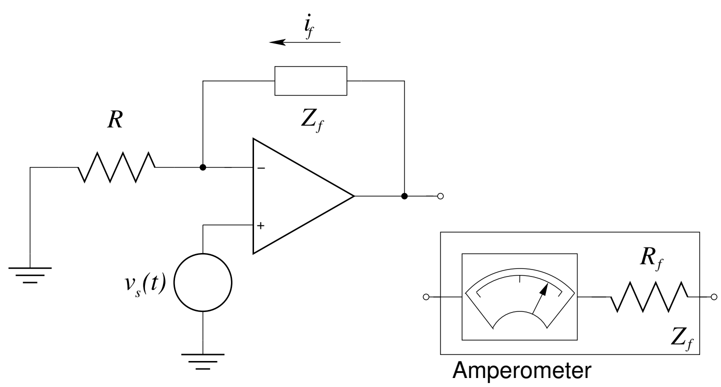


Figure 5.3: Basic transconductance amplifier circuit.

The current flowing through the impedance Z_f is proportional to the voltage v_s. In fact, supposing the infinite input impedance of the Op-Amp, we will have

$$i_f(t) = \frac{v_s(t)}{R_f}.$$

Placing an amperometer in series with a resistor with large resistance as a feedback impedance, we will have a high resistance voltmeter. In other words, the induced perturbation of such circuit will be very small because of the very high impedance of the operational amplifier.

5.1.4 Current to Voltage Converter (Transresistance Amplifier)

A current to voltage converter is an amplifier that produces a voltage proportional to the input current. The constant of proportionality is called *transimpedance* or *transresistance*, whose units are Ω. Figure 5.4 show a basic configuration for a transimpedance Op-Amp. Due to the virtual ground the current through the shunt resistance is zero, thus the output voltage is the voltage difference across the feedback resistor R_f, i.e.

$$v_o(t) = -R_f\, i_s(t).$$

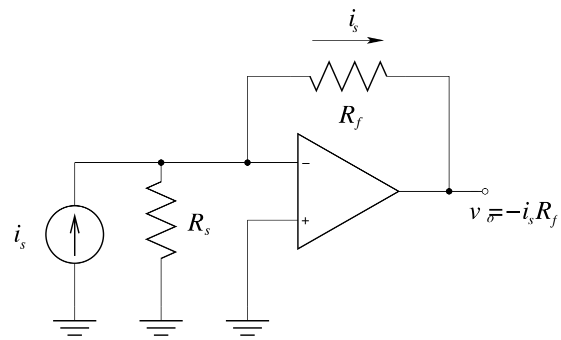


Figure 5.4: Basic transimpedance Op-Amp.

Photo-multipliers photo-tubes and photodiodes drivers are a typical application for transresistance Op-amps. In fact, quite often the photocurrent produced by those devices need to be amplified and converted into a voltage before being further manipulated.

5.2 Logarithmic Circuits

Combining logarithmic circuits such as logarithmic and anti-logarithmic amplifiers we can implement analog multipliers and dividers. Let's see in more details how those circuit work.

For improved logarithmic circuits consult [1] chapter 7, and and [1] section 16-13.

5.2.1 Logarithmic Amplifier

Figure 5.5 shows an elementary logarithmic amplifier, i.e. the output is proportional to the logarithm of the input. A BJT as feedback provides a larger input dynamic range. Let's analyze the logarithmic amplifier in more detail.

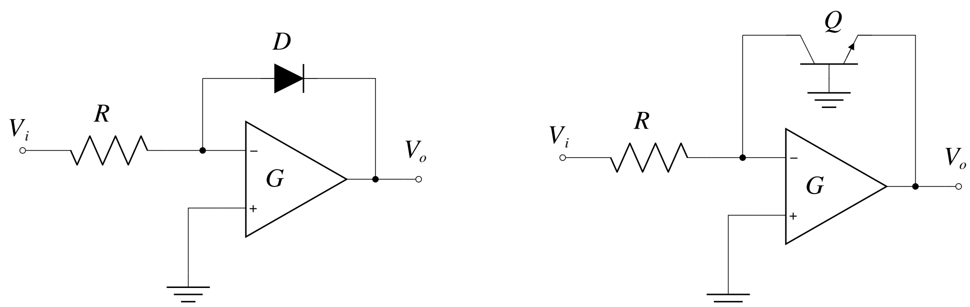


Figure 5.5: Elementary logarithmic amplifier

Because the Op-Amp is mounted as an inverting amplifier, if v_i is positive, then v_o must be negative and the diode is in conduction.

We must have

$$i \simeq I_s e^{-qV_o/k_B T} \qquad I_s \ll 1,$$

where $q < 0$ is the electron charge. Considering that

$$i = \frac{v_i}{R},$$

and after some algebra we finally get

$$v_o = \frac{k_B T}{-q} \left[\ln(v_i) - \ln(RI_s) \right] .$$

The constant term $\ln(RI_s)$ is a systematic error that can estimated and subtracted at the output. It is worth to notice that v_i must be positive to have the circuit working.

5.2.2 Anti-Logarithmic Amplifier

Figure 5.6 shows an elementary logarithmic amplifier, i.e. the output is proportional to the inverse of logarithm of the input. Same remarks of the logarithmic amplifier about the npn BJT applies to this circuit.

The current flowing through the diode or the BJT is

$$i \simeq I_s e^{-qV_i/k_B T} \qquad I_s \ll 1,$$

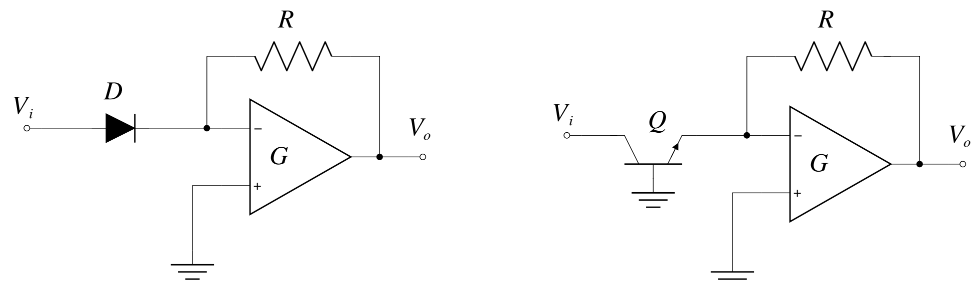


Figure 5.6: Elementary anti-logarithmic amplifier

where in the argument of the exponential function we have the input voltage. Considering that

$$v_o = -Ri\,,$$

thus

$$v_o \simeq -RI_s e^{-qV_i/k_BT}.$$

If the input v_i is negative, we have to reverse the diode's connection or replace the BJT with a pnp BJT.

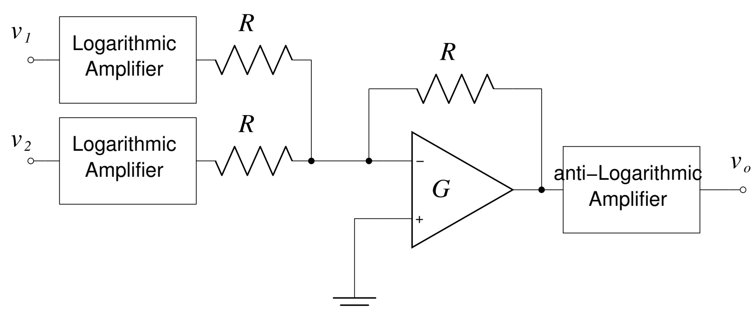


Figure 5.7: Elementary analog multiplier.

5.2.3 Analog Multiplier

Figure 5.7 shows an elementary analog multiplier based on a two log one anti-log and one adder circuits. Fore more details about the circuit see [1] section 7-4 and [1] section 16-13.

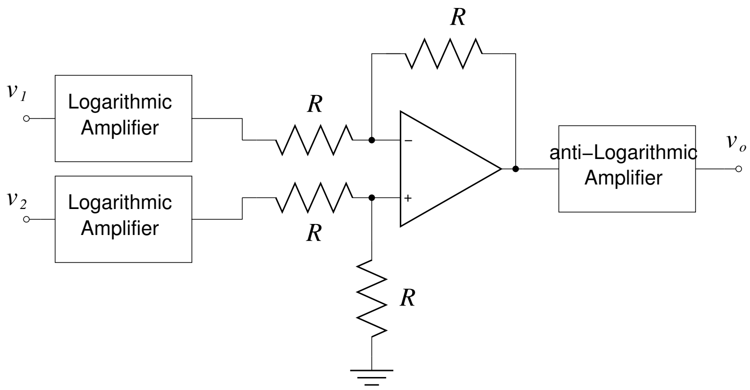


Figure 5.8: Elementary analog divider.

5.2.4 Analog Divider

Figure 5.7 shows an elementary logarithmic amplifier based on a two log one anti-log and one adder circuits. Fore more details about the circuit see [1] section 7-5 and [1] section 16-13.

5.3 Multiple-Feedback Band-Pass Filter

Figure 5.9 shows the so called multiple-feedback bandpass, a quite good scheme for large passband filters, i.e. moderate quality factors around 10.

Here is the recipe to get it working. Select the following parameter which define the filter characteristics, i.e the center angular frequency ω_0 the quality factor Q or the the passband interval (ω_1, ω_2) , and the passband gain A_{pb}

$$\begin{aligned} \omega_0 &= \sqrt{\omega_2 \omega_1} \\ Q &= \frac{\omega_0}{\omega_2 - \omega_1} \\ A_{pb} &< 2Q^2 \end{aligned}$$

Set the same value C for the two capacitors and compute the resistance values

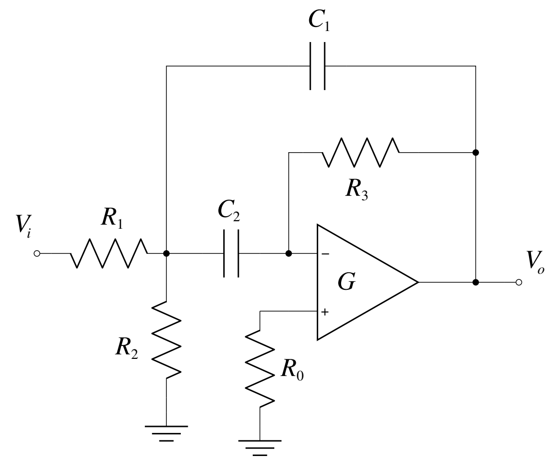


Figure 5.9: Multiple-feedback band-pass filter.

$$
\begin{aligned}
R_1 &= \frac{Q}{\omega_0 C A_{pb}} \\
R_2 &= \frac{Q}{\omega_0 C \left(2Q^2 - A_{pb}\right)} \\
R_3 &= \frac{Q}{\omega_0 C}
\end{aligned}
$$

Verify that

$$A_{pb} = 2\frac{R_3}{R_1} < 2Q^2$$

See [1] sections 8-4.2, and 8-5.3 for more details.

5.4 Peak and Peak-to-Peak Detectors

The peak detector circuit is shown in figure 5.10. The basic ideal is to implement an integrator circuit with a memory.

To understand the circuit let´s first short circuit D_o and remove R. Then the Op-amp A_0 is just a unitary gain voltage follower that charges the capacitor C up to the peak voltage. The function of D_0 and if A_1(high input impedance) is to prevent the fast discharge of the capacitor.

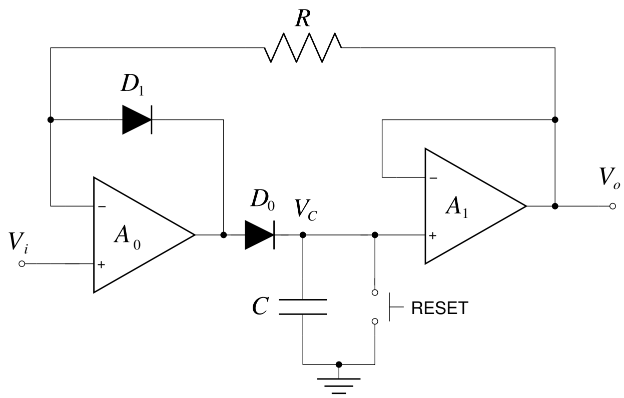


Figure 5.10: Peak detector circuit.

Because of D_0 the voltage across the capacitor is not the max voltage at the input, and this will create a systematic error at the output V_o.Placing a feedback from $V_o$to V_i will fix the problem. In fact, because V_+must be equal to V_-, A_0 will compensate for the difference.

Introducing the resistance ($R \simeq 100\text{k}\Omega$) in the feedback will provide some isolation for V_o when V_i is lower than V_C.

The Op-Amp A_0 should have a high slew rate (at least ~20 V/μs) to avoid the maximum voltage being limited by the slew rate.

The capacitor doesn´ t have to limit the Op-Amp A_0 slew rate S, i. e.

$$\frac{i_C}{C} \ll \frac{dV}{dt} = S$$

It is worthwhile to notice that if D_0 and D_1 are reversed the circuit becomes a negative peak detector.

Using a positive and a negative peak detector as the input of a differential amplifier stage we can build a peak-to-peak detector (for more details see [1] section 9-1).

5.5 Zero Crossing Detector

When $v_i$is positive and because it is connected to the negative input then v_o becomes negative and the diode $D_1$is forward biased and conducting..

5.6 Analog Comparator

An *analog comparator* or simply *comparator* is a circuit with two inputs v_i, v_{ref} and one output $v_o$which fulfills the following characteristic:

$$v_o = \begin{cases} V_1 & , v_i > v_{ref} \\ V_2, & v_i \leq v_{ref} \end{cases}$$

An Op-Amp with no feedback behaves like a comparator. In fact, if we apply a voltage $v_i > v_{ref}$, then $V_+ - V_- = v_i - v_{ref} > 0$. Because of the high gain, the Op-Amp will set v_o to its maximum value $+V_{sat}$which is a value close to the positive voltage of the power supply. If $v_i < v_{ref}$, then $v_o = -V_{sat}$. The magnitude of the saturation voltage are typically about 1V less than the supplies voltages.

Depending on which input we use as voltage reference v_{ref}, the Op-amp can be an inverting or a non inverting analog comparator.

5.7 Regenerative Comparator (The Schmitt Trigger)

The *Regenerative comparator* or *Schmitt Trigger* shown in figure 5.11 is a comparator circuit with hysteresis.

It is worthwhile to notice that the circuit has a positive feedback. With positive feedback, the gain becomes larger than the open loop gain making the comparator swinging faster to one of the saturation levels.

Considering the current flowing through R_1 and R_2,we have

$$I = \frac{V_1 - V_+}{R_2} = \frac{V_+ - V_o}{R_1}, \qquad \Rightarrow \qquad V_+ = \frac{V_1 R_1 + V_o R_2}{R_1 + R_2} .$$

The output V_o can have two values, $\pm V_{sat}$. Consequently, V_+will assume just two trip points values

$$V_+^{(utp)} = \frac{V_1 R_1 + V_{sat} R_2}{R_1 + R_2} \qquad V_+^{(ltp)} = \frac{V_1 R_1 - V_{sat} R_2}{R_1 + R_2}$$

When $V_i < V_+^{(utp)}$, V_o is high, and when $V_i < V_+^{(ltp)}$, V_o is low.

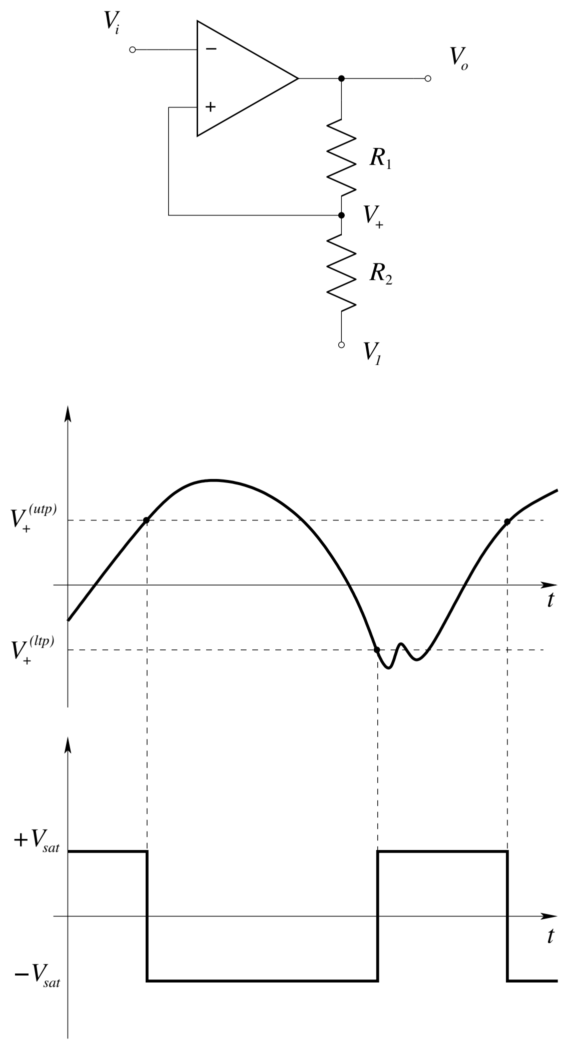


Figure 5.11: Schmitt Trigger.

To set $V_+ = 0$ it requires that

$$V_1 = -\frac{R_2}{R_1} V_o$$

This circuit is usually used to drive an analog to digital converter (ADC). In fact, jittering of the input signal due to noise which prevents from keeping the output constant, will be eliminated by the hysteresis of the Schmitt trigger (values between the trip points will not affect the output).

See [1] section 11 for more detailed explanations.

Example1: ($V_{sat} = 15$V)

Supposing we want to have the trip points to be $V_+ = \pm 1.5V$, if we set $V_1 = 0$ then $R_2 = 9R_1$.

5.8 Phase Shifter

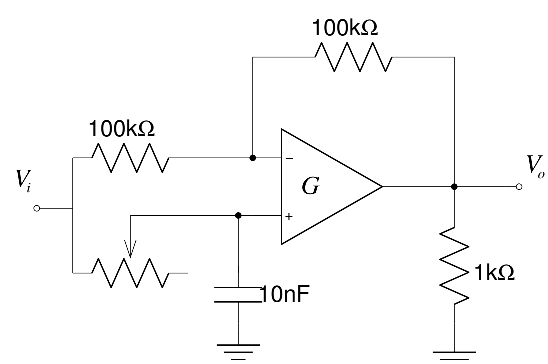


Figure 5.12: Phase shifter circuit.

A phase shifter circuit shown in figure 5.12, produces a signal at the output V_o which is equal to the input V_i with a phase shift φ given by the following formula

$$\tan\left(\frac{|\varphi|}{2}\right) = \frac{1}{RC\omega}$$

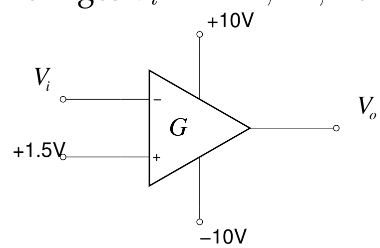
Supposing that we want a phase shift of $90^o$for a 1kHz sinusoid , then

$$R = \frac{1}{\tan\left(\frac{\varphi}{2}\right) C\omega} = \frac{1}{1 \cdot 10^{-8} \cdot 2\pi \cdot 10^3} = 15.915\mathrm{k}\Omega.$$

Exchanging the potentiometer and the capacitor changes lead to lag.

5.9 Problems Preparatory to the Laboratory

1. Considering the following circuit, determine the voltage output V_o for the following input voltages $V_i = -2\text{V}, 1\text{V}, 1.5\text{V}, 3\text{V}$



2. Consider the Schmitt trigger of figure 5.11.

   (a) If $V_o = -15\text{V}$ and $V_+ = 0\text{V}$, compute V_1.

   (b) If $V_o = +15\text{V}$, and $V_1 = 15\text{V}$, compute V_+.

3. Design a Schmitt trigger with two diode clamps and one resistor connected to the output.

   (a) Limit the output V_o from 0 to 5V.

   (b) Compute the resistance value R necessary to limit the diode current to 10mA.

4. Chose at least two circuit to study and design.
   New circuits different than those ones proposed in this chapter are also welcome. For a good source of new circuits based on Op-Amps see [1] , [2], and [1].

5.10 Laboratory Procedure

No special procedure is required for this laboratory week. The student is encouraged to study, build and test more than one circuit (two at least). It is important also to try to find out limitations and measure the performance of each single circuit. Students are also encouraged to try basic Op-Amp applications different from the ones suggested in this notes.

As usual, a report of the work done during the laboratory hours is required.

Consult the data-sheet to properly connect the devices pin-out.

Before powering your circuit up, always cross-check the power supply connections. It is always a good practice to turn on the dual power supply at the same time to avoid potential damages of electronic components.

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Chapter 6

Basics on Oscillators

6.1 Introduction

Waveform generators are essentially circuits which provide a periodic signal with constant frequency, phase, and amplitude. The quality of these devices are measured by the frequency, and amplitude stability and absence of distortion. The last characteristics is essentially cleanness of the spectrum signal. For example, the spectrum of a perfect sinusoidal oscillator must be a delta of Dirac at the oscillating frequency. Practically, sinusoidal oscillators has a sharp narrow peak at the oscillation frequency, and other less taller peaks at different frequencies, mainly at multiples of the oscillation frequency (harmonics).

In this chapter we will study the criterion to sustain a sinusoidal oscillation with a positive feedback amplifier, the so-called **Barkhausen criterion**, and some simple circuit to produce different wave forms.

6.2 Criterion for Sinusoidal Oscillation (Barkhausen Criterion)

Let's consider an amplifier with a positive feedback network as show in figure 6.1. Considering that the summation point output is

$$V_i + \beta(\omega)V_o,$$

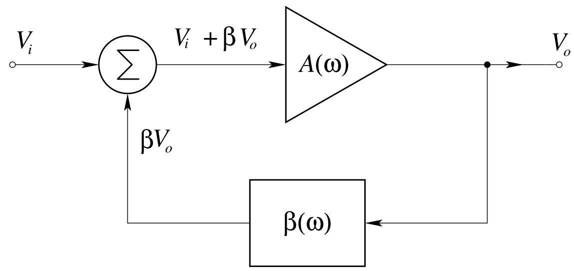


Figure 6.1: Amplifier with positive feedback

and the amplifier gain is $A(\omega)$, the output voltage will be

$$V_o = A(V_i + \beta V_o),$$

Collecting V_o we will finally have

$$V_o = \frac{A}{1 - \beta A} V_i.$$

For

$$|\beta(\omega)A(\omega)| = 1, \qquad \arg\left[\beta(\omega)A(\omega)\right] = 0, 360, ...$$

the output V_o diverges. Supposing that the previous condition is satisfied for a given angular frequency ω_0, any excitation at the frequency ω_0 will make the output to oscillate at the frequency ω_0 with an undefined amplitude. The previous condition which can be rewritten as

$$\Re[\beta A] = -1, \qquad \Im[\beta A] = 0$$

is the so called **Barkhausen criterion** for the oscillation.

The term βA is called the **loop gain** since that is exactly the gain of the loop in the feedback amplifier network. Sometimes, it is also called **open loop gain.**

6.2.1 Practical Considerations

Oscillators with exactly unitary loop gain and $V_i = 0$ are just a mere abstraction. Moreover, drifts due to temperature and aging would make this condition impossible to keep.

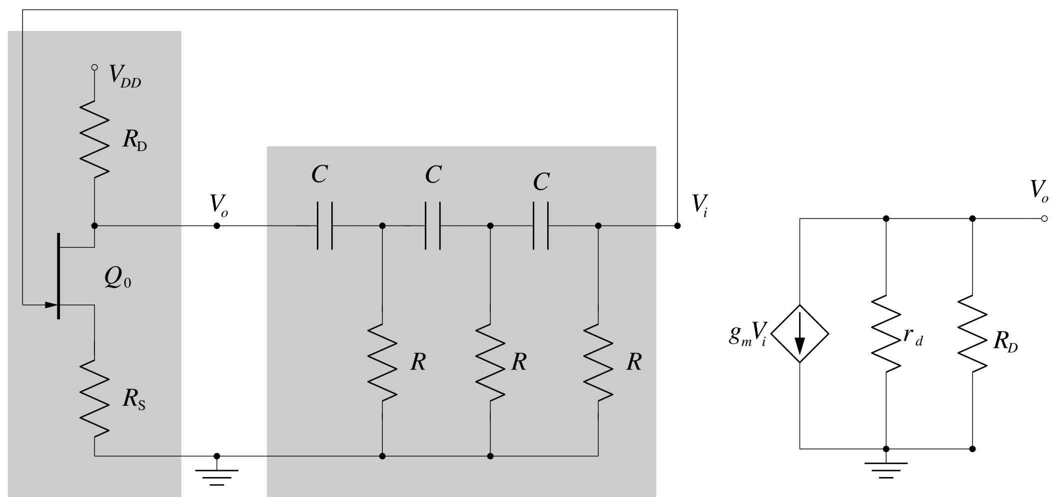


Figure 6.2: Phase shift oscillator using a JFET as amplification stage (left gray rectangle) and a phase shift network (right gray rectangle). The circuit on the left represents the low frequency model of the JFET amplifier.

Practically, it is necessary to have a loop gain somewhat larger than unity ($A\beta \simeq 1.05$) to sustain the oscillation. This can lead to a slow drift of the oscillation amplitude which can produce a saturation effect.

Large values of the amplifier gain A produce saturation at the output and can be used to generate squares or pulse waves.

It is important to notice that we don't have to provide an initial kick to start the oscillation. This is true, because every time we switch a circuit on a step propagates through the circuit providing an initial excitation at the right frequency. Moreover, the probability to have a small signal fluctuation at the right frequency are usually quite high.

The frequency stability of the oscillator depends mainly on the ability of the circuit to maintain the loop gain phase constant to $0°$or multiple of $360°$.

In the discussion of some oscillator circuits we will assume that the amplifier is able to deliver the required positive or negative gain without adding any additional phase. In the general case, this is clearly a crude approximation, but it is used just to simplify the study of the circuits.

6.3 Phase Shift Oscillator

The phase shift oscillator exemplifies the concepts set forth above. Referring to figure 6.2, we can distinguish the JFET amplifier stage and the positive feedback network made of three cascaded RC phase shifting filters.

Supposing that the amplifier load Z_L is negligible, i.e. $|Z_L| \gg R_D||r_d$ then, the amplifier will just change sign $(180°)$ to any signal injected in the gate. The network feedback will provide additional phase shift to satisfy the Barkhausen criterion at a given angular frequency ω_0.

It can be proved that

$$\beta(\omega) = \frac{V_i}{V_o} = \frac{1}{1 + \frac{5}{(\omega\tau)^2} + j\left(\frac{1}{(\omega\tau)^3} - \frac{6}{\omega\tau}\right)} \qquad \tau = RC\ , \tag{6.1}$$

The amplifier gain, supposed to be constant is $A = -g_m R_D$, where g_m is the JFET amplifier gain.

Imposing the condition $\Im[\beta A] = 0$, we get

$$\omega_0 = \frac{1}{\sqrt{6}}\frac{1}{\tau}.$$

Replacing the previous expression in the open loop gain $A\beta$ and using the second condition $\Im\left[\beta A\right] = -1$, we get

$$g_m R_D = 29$$

To sustain the oscillation, the amplifier must have a gain of at least $29/R_D$.

6.4 The Wien Bridge Oscillator

The Wien Bridge Oscillator show in figure 6.3, uses a differential amplifier to provide positive and negative feedback to satisfy the two condition of oscillation.

Referring to figure 6.3 , setting $Y_C = 1/\left(j\omega C\right)$, and thanks to the voltage divider equation we can write

$$V_+ = \frac{\frac{RY_C}{Y_C+R}}{R + Y_C + \frac{RY_C}{Y_C+R}}V_o = \frac{1}{\frac{(Y_C+R)^2}{RY_C} + 1}V_o = \frac{1}{\frac{Y_C}{R} + \frac{R}{Y_C} + 3}V_o$$

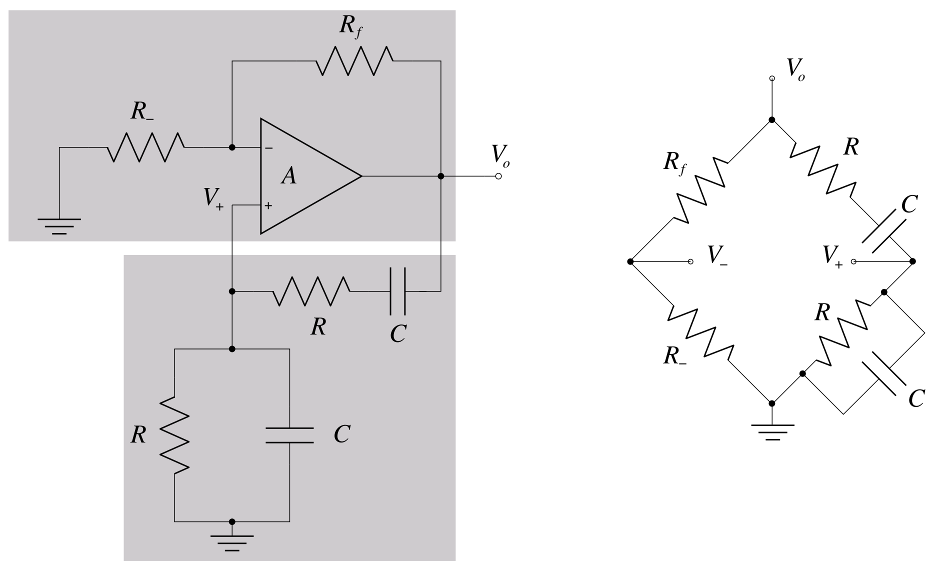


Figure 6.3: Wien bridge oscillator, and components rearrangement to show the bridge topology.

and

$$\beta(\omega) = \frac{V_+}{V_o} = \frac{1}{3 + j\left(\omega\tau - \frac{1}{\omega\tau}\right)} \qquad \tau = RC.$$

The oscillation will happen where the phase shift is zero, i.e. for

$$\omega\tau - \frac{1}{\omega\tau} = 0, \qquad \Rightarrow \qquad \omega_0 = \frac{1}{\tau}\,.$$

The angular oscillation frequency ω_0 depends on the inverse of the resistance R and the capacitance C.

Because the attenuation at the resonant frequency is

$$\frac{V_+}{V_o} = \frac{1}{3}\,.$$

the negative feedback must have a theoretical gain of $A(\omega_0) = 3$. The resistances R_- and R_f must be given by the usual equation

$$\frac{V_{o'}}{V_+} = 1 + \frac{R_f}{R_-}\,.$$

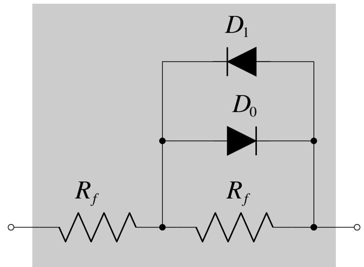


Figure 6.4: Automatic gain control circuit for the Wien bridge oscillator negative feedback.

The oscillation frequency can be continuously tuned using coupled variable resistors.

To minimize distortions due to the Op-amp saturation when the gain is larger than one, it is required to provide a circuit with variable gain. Essentially, we need an overall gain larger than one for small signal to sustain the oscillation and gain of about 1 or less for large signal to avoid distortion. The negative feedback path shown in figure 6.4 does the job. For large signals the one diodes becomes forward biased reducing the feedback resistance and the Op-Amp gain. For smaller signal the gain is not affected by the diodes.

Practically, Wien Bridge oscillators are used in the kilohertz region with a variable range up to ~10 times ω_0.

6.5 LC Oscillator

A quite general form of oscillator circuits is depicted in figure 6.6. Let's suppose that the amplifier is ideal but has a non zero output resistance R_o. Referring to figure 6.6, and using the voltage divider equation we have

$$V_o = -\frac{Z_L}{R_o + Z_L} A V_-, \qquad Z_L = Z_2 || \left(Z_1 + Z_3\right) \ .$$

After some algebra we get

$$\beta = -\frac{Z_1 Z_2}{R_o \left(Z_1 + Z_2 + Z_3\right) + Z_2 \left(Z_1 + Z_3\right)} \ . \tag{6.2}$$

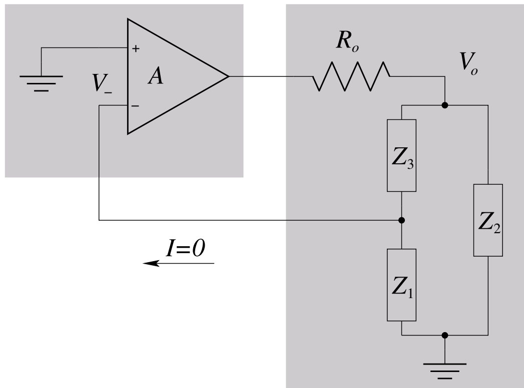


Figure 6.5: LC Oscillator circuit. The resistance R_o is the output impedance of the Op-Amp.

Let's consider the case of the LC tunable oscillators, i.e. the impedances are purely reactive (real part equal to zero)

$$Z_i = jX_i \,, \qquad X_i > 0 \qquad \text{for } i = 1, 2, 3$$

Then the previous formula becomes

$$\beta = \frac{X_1 X_2}{jR_o\,(X_1 + X_2 + X_3) - X_2\,(X_1 + X_3)} \,.$$

For β to be real

$$X_1 + X_2 + X_3 = 0 \,,$$

and

$$\beta(\omega_0) = -\frac{X_1}{X_1 + X_3} \,,$$

where ω_0 is the oscillation frequency. Using the two previous equation we finally get

$$\beta(\omega_0) = \frac{X_1}{X_2} \,.$$

Since $\beta(\omega_0)$ must be positive, $X_1$and X_2 must have the same sign, which means that they have to be the same kind of reactance, two capacitors or two inductors. From the condition of imaginary part equal to zero we

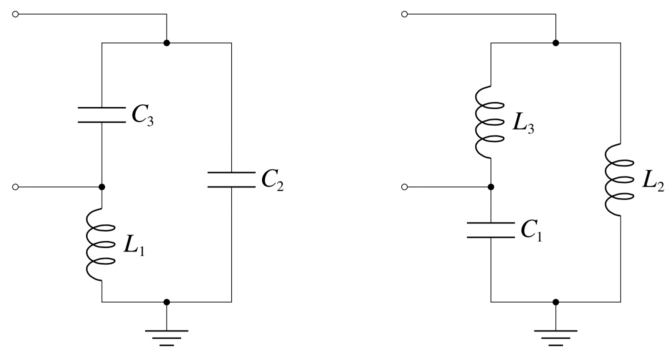


Figure 6.6: Colpitts (left) and Hartley (right) feedback circuits $\beta(\omega)$ for the LC oscillator circuit.

find that if X_1 and X_2 are capacitors X_3 must be an inductor, and vice versa. Here is the oscillator circuit name depending on the choice of the reactance:

- **Colpitts Oscillator**: X_1 and X_2 capacitive reactances and X_3 an inductive reactance ($X_{1,2} = -1/(\omega C_{1,2})$, $X_3 = \omega L_3$).
  The oscillator angular frequency and the gain in this case are

$$\omega_0 = \sqrt{\frac{1}{L_3\left(\frac{C_1 C_2}{C_1+C_2}\right)}}, \qquad \beta(\omega_0) = \frac{C_2}{C_1}$$

- **Hartley oscillator**: X_1 and X_2 inductive reactances and X_3 a capacitive reactance ($X_{1,2} = \omega L_{1,2}$, $X_3 = -1/(\omega C_3)$).
  The oscillator angular frequency and the gain in this case will be

$$\omega_0 = \sqrt{\frac{1}{C_3\left(L_1 + L_2\right)}}, \qquad \beta(\omega_0) = \frac{L_1}{L_2}$$

Using a BJT amplifier we can usually obtain higher oscillating frequency than using standard operational amplifiers. In this case the high frequency hybrid-π model[1] must be used to properly model the transistor behavior.

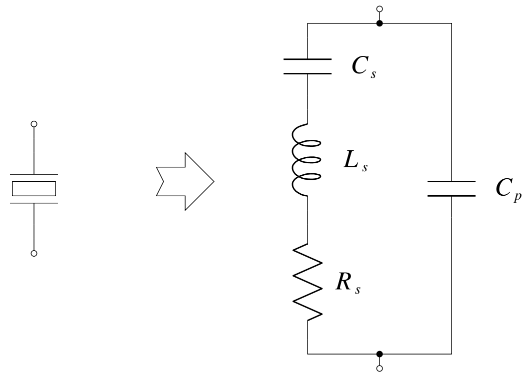


Figure 6.7: Circuit symbol for a piezoelectric oscillator (or quartz oscillator) and the equivalent electronic circuit. The LCR series circuit accounts for the sharp mechanical resonance The capacitor $C_p$in parallel describes the capacitance of the crystal for frequency far for the resonance.

6.6 Crystal Oscillator

Crystal oscillators are based on the property of piezoelectricity[1] exhibited by some crystals and ceramic materials. Piezoelectric materials change size when an electric field is applied between two of its faces. Conversely, if we apply a mechanical stress, piezoelectric materials generate an electric field. Some crystals have internal mechanical resonances with very high quality factors (quartz can reach quality factors of 10^4) [2] and can be indeed used to generate very stable oscillators.

Figure 6.7 shows the circuit symbol for a piezoelectric component and the equivalent circuit modeled using ideal components.

Usually, to apply an electric field to a crystals is necessary to make a conductive coating on two parallel faces, and this process creates a capacitor with an interposed dielectric. This explain the presence of the capacitor of capacitance C_p in the model. The LCR series circuit accounts for the par-

[1]Piezoelectricity was discovered by Jacques and Pierre Curie in the 1880's during experiments on quartz.

[2]Mechanical resonance stability depends mainly on the fact that the resonance value is determined by the crystal geometry. It the crystal size slightly depends on the temperature we can have very stable resonators. Active temperature stabilization can clearly improve frequency stability.

ticular mechanical resonance we want to use to build the oscillator.

To design a crystal oscillator it is important to study the reactance (the imaginary part of the impedance) whose qualitative behavior is shown in figure ?? . Where the reactance is essentially inductive and very close to the resonance, the crystal behaves as a simple equivalent inductor. We can indeed replace the inductor L_s of the LC oscillator of figure 6.6 with the piezoelectric crystal to build a simple oscillator.

Crystal oscillators using a Colpitts configuration and a BJT in common-emitter or common-collector configuration, can work from few kHz up to ~100MHz.

6.7 Charge and Discharge Oscillator (Relaxation Oscillator)

TBD

6.8 Problems Preparatory to the Laboratory

1. Replace a JFET amplifier of the phase shift oscillator with an Op-amp. Hint: the amplifier configuration must provide $180°$ of phase shift and the virtual ground can be used to simplify the feedback network and amplifier.
   Find the components values to satisfy the Barkhausen criterion for an oscillating frequency $\nu = 5$kHz.

2. Design a Wien bridge oscillator with a frequency of 1kHz, 5kHz and 10kHz.

3. Derive the expression 6.2 of $\beta(\omega)$ for the LC oscillator.

6.9 Laboratory Procedure

Read carefully the entire procedure before starting the experiment.

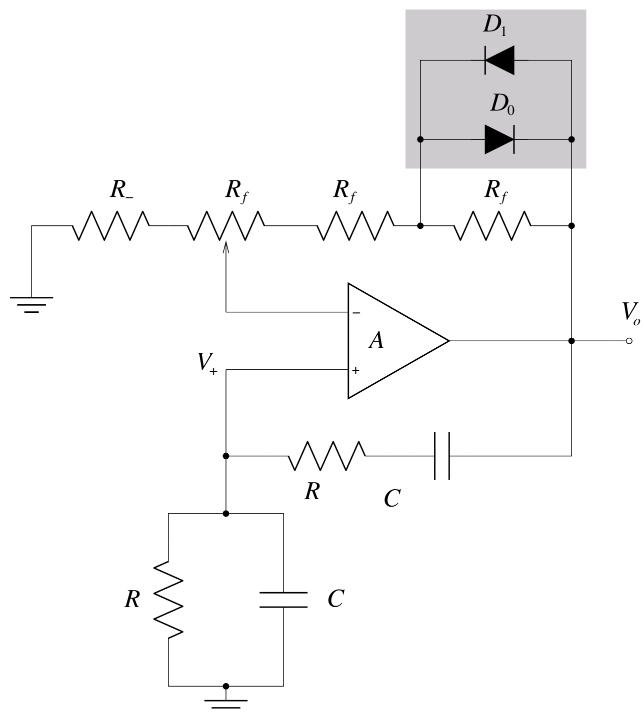
Consult the data-sheet to properly connect the devices pin-out.

Before powering your circuit up, cross-check the power supply connections.

It is always a good practice to turn on the dual power supply at the same time to avoid potential damages of circuit components.

Note on your log book all the unpredicted behavior you experience in the circuits response.

1. Build a Wien bridge sinusoidal oscillator with a frequency ν between 1kHz and 10kHz with a μ741 Op-Amp. Use a potentiometer to match the resistances of the positive feedback network. Arrange more than one capacitor to obtain two capacitances with the same value. Neglect first the automatic gain control circuit highlighted in the gray box in the figure below



   (a) Measure the open loop transfer function $A(\omega)\beta(\omega)$ to verify the gain and phase around the resonance.
   (b) Compare the measured oscillator frequency $\langle\omega_0\rangle_{Exp}$with the theoretical value ω_0.
   (c) Check the behavior of the circuit when the open loop gain $A\beta$ is greater than one or smaller than one

(d) Add the AGC circuit and tune the gain to properly sustain the oscillation.

(e) Verify that the oscillator can be tuned by changing the resistors or the capacitors pair.

(f) Measure the spectrum of your oscillator using a spectrum analyzer, and compute the total harmonic distortion

$$THD = \frac{1}{V_0^2}\sum_{n=1}^{N} V_n^2 ,$$

where V_n is the amplitude of the *nth*-harmonic frequency. N is determined by the resolution of the instrument and the required precision.

Bibliography

[1] Microelectronics, Jacob Millman, and Arvin Grabel , Mac-Graw Hill

Appendix A

Fourier Analysis

A.1 Discrete Spectrum

The Fourier analysis is a fundamental an extremely useful method to characterize a generic signal. It is based on the Fourier theorem which states[1] that any periodic function $v_T(t)$ can be represented as a series of sines with different amplitudes V_n , and frequency $\omega = n\omega_0$, i.e.

$$v_T(t) \;\; = \;\; \sum_{n=0}^{\infty} V_n \sin\left(\omega_0 n t\right), \quad \omega_0 = \frac{2\pi}{T}\,.$$

The set of points (ω, V_n) is called discrete spectrum of the function and is given by the following integrals

$$V_n = \frac{2}{T}\int_0^T v_T(t)\sin\left(\omega_0 n t\right) dt.$$

A.1.1 Example: Square Wave

If we consider a square wave symmetric respect to the time axis

$$v_T(t) = \begin{cases} v_0, & 0 \le t < T/2 \\ -v_0, & T/2 \le t < T \end{cases}\;,$$

then the corresponding Fourier series is

$$v_T(t) = \sum_{i=0}^{\infty} \frac{4v_0}{\pi}\frac{1}{2n+1}\;\sin\left[(2n+1)\omega_0 t\right]\;.$$

[1]Here the Fourier series theorem is not enunciated in its most general form.

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Figure A.1: Time domain representation (left) and frequency domain representation (right) of a square wave signal.

Figure A.1 shows the time domain representation of the signal and its frequency domain representation or frequency spectrum.

A.2 Continuous Spectrum

Using Fourier transform operator, the representation in the frequency domain can be extended to any type of signal $v(t)$

$$v(t) = \int_{-\infty}^{+\infty} V(\omega) e^{i\omega\tau} d\omega$$

and in this case we will have a continuum spectrum given by the Fourier integral

$$V(\omega) = \frac{1}{2\pi} \int_{-\infty}^{+\infty} v(t) e^{-i\omega\tau} d\tau.$$

It is important to notice that $v(t)$ can be any type of signal even a random signal, in other words a noise. Real signals can be considered as the sum of deterministic and random signals. If we compute a spectrum of such a signal we expect to see the contribution of both, i.e. the noise spectrum which is present at all frequencies and the signal spectrum.

A.2.1 Spectrum Estimation

For practical purposes, the spectrum is always estimated in a finite interval, (nobody can wait that long to compute a spectrum). The signal is

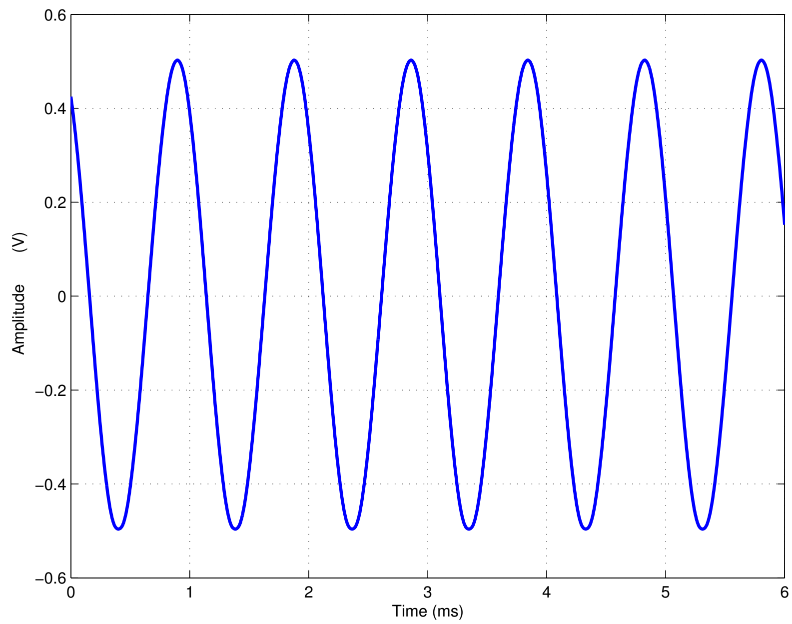

Figure A.2: Sinusoidal signal produced by a function generator (Tektroniχ GFG253) and acquired using a Spectrum analyzer (Stanford SR785).

acquired using an analog to digital converter and then numerically processed using the fast Fourier transform algorithm to estimate the spectrum. The results is a truncated discrete spectrum, which estimates the signal continuous spectrum.

A.2.2 Power Spectral Density and Units

The square of the Fourier coefficients $|V(\omega)|^2$, which are proportional to the signal power are calculated to estimate the signal spectrum. Normalizing those coefficients by the frequency step size (bin) of the discrete spectrum we obtain the so called *power spectral density* (PSD). This operation is mainly done to allow the amplitude comparison of spectra taken with different bins. In this case, the coefficients units are

$$\left[|V(\omega)|^2\right] = \frac{\text{[power arbitrary units]}}{\text{Hz}}.$$

Quite often, the square root of the PSD is considered, and unfortunately, it is quite common to find scientists who inaccurately call it PSD.

A.2.3 Example: Sinusoidal Function Generator

Figure A.2 shows a sinusoidal signal produced by a function generator and acquired with a digital instrument called spectrum analyzer. The frequency spectrum computed using the same instrument, is shown in figure A.3. The lower plot of figure A.3 shows the same spectrum between 500Hz and 10kHz with a horizontal linear scale to emphasize the harmonics content.

If we look at the time domain, it is quite difficult to see any harmonic distortion of the signal. On the contrary, the frequency domain representation clearly shows all the signal distortions.

The fundamental frequency is $\nu_0 = 1.02$kHz and the amplitude is $V_0 = 0.26$V/$\sqrt{\text{Hz}}$. The next harmonic, the second taller peak, has an amplitude $V_1 = 0.8$mV/$\sqrt{\text{Hz}}$, which implies that the fundamental frequency amplitude is at least more than 300 times larger than each high order harmonics.

Considering the time domain plot, the amplitude of the sinusoid is $V_0 = 0.5V_{pk}$, then the frequency bin amplitude must be $\Delta\nu = 3.7$Hz $(0.5/\sqrt{3.7} = 0.26$V/$\sqrt{\text{Hz}})$.

The spectrum also shows several peaks symmetric around the fundamental frequency ν_0 due to unwanted amplitude modulations of the fundamental frequency.

The other feature visible in the spectrum is the noise floor, i.e the noise level around the peaks base. This noise floor is reasonably flat above ν_0 with a magnitude $\delta V \simeq 0.2 - 0.3\mu$V/$\sqrt{\text{Hz}}$. Below ν_0 seems to have a negative slope and an average value of $\delta V \sim 0.7\mu$V/$\sqrt{\text{Hz}}$.

The so called power lines (60Hz and harmonics) are clearly visible in the spectrum.

In general, it is important to know and measure the resolution of the instrument to be certain that the noise level measurement is not dominated by the instrument noise. Moreover, the instrument resolution depends on the input dynamic range. The larger is the dynamic range the worst is the instrument resolution. Quite often, the dynamic range can be reduced removing the DC component of the signal to measure. In this particular case, a better resolution could be achieved reducing the dynamic range with a notch filter tuned at the frequency ν_0.

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Figure A.3: Sinusoidal signal spectrum of figure A.2. Upper plot shows the spectrum with a logarithmic scale for the horizontal axis. The lower plot uses a linear scale between 500Hz to 10kHz.

Appendix B

Impedance Models for Passive Components

A more realistic frequency dependent model of passive components can be achieved considering equivalent circuits made of ideal passive components or components whose impedance depends on the frequency.

As a general remark, we can say that this kind of representation strongly depends on the technology used to manufacture the electronics devices and on the frequency range.

The particular equivalent circuit of a real component allows us to take into account physical mechanism of the conduction in the passive component such as the conductor the skin [**?**] effect, the proximity effect, and dissipation phenomena of dielectrics.

For example, the skin effect arises with AC currents. In this case the current density is not uniform across the conductor cross section. For a conductor with a circular cross section the current density $J(r)$ measured at a distance r form the conductor surface is

$$J(r, \omega) = J_0 e^{-r/\delta(\omega)}$$

where J_0 is the current density on the surface and $\delta(\omega)$ an effective distance which goes like $1/\sqrt{\omega}$ and depends on the type of conductor. The expected resistance R of the conductor

$$R(\omega) = \frac{V}{2\pi \int J(r, \omega) dr},$$

is indeed not constant as a function of the frequency.

The proximity effect arises when two or more conductors are close enough that their varying electromagnetic fields perturbs the currents in the adjacent conductors. This effect depends on the geometry of the system and on the frequency of the currents, i.e of the electromagnetic fields.

B.1 Resistor

The realistic model of a resistor of nominal resistance R is shown in figure B.1. This is particularly important when the resistance is made out of a resistive wire.

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Figure B.1: Equivalent representation of a resistor with nominal resistance R using ideal components.

The ideal passive components are needed to model the following mechanisms:

- R The resistance measured across the resistor in the DC regime.
- L_s The inductance of the wires. If the resistor is a coil, the inductance is clearly not negligible at high frequency .
- C_p The capacitance of the wire. if the resistor is a coil, the capacitance at high frequency is essentially due to the capacitance among the windings,

Up to 100MHz, the common used carbon dioxide resistors, have negligible values of L_s and C_p. Their more important constraint is the maximum dissipated power, which cannot exceed few watts. common high dissipating resistors are made of a spooled resistive wire .

B.2 Capacitor

Two more realistic models of a capacitor of nominal capacitance C, is shown in figure B.2.

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Figure B.2: Starting from left, the ideal capacitor, the high frequency model for a capacitor (typically above 20MHz) , and the low frequency model (below 20MHz).

The ideal passive components are needed to model the following mechanisms:

- C the capacitance measured across the capacitor in the DC regime.
- R_s The resistance due electric contacts, solder , etc.
- L_s The inductance due to the leads.
- $R_p(\omega)$ The resistance of the dielectric used to build the capacitor which depends on the frequency.

Quite often, for frequencies below about 20MHz, L_s and R_s can be neglected. In this case, to characterize the capacitor it is used to the define the so called loss angle ϕ (see figureB.3) defined as

$$\phi = \arctan\left(R_p C\,\omega\right)$$

which is the complementatry angle of the sum of the current I_{R_p}, and I_C. If $\phi = 0$ the capacitor is ideal.

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Figure B.3: Definition of the capacitior loss angle. If $\phi = 0$ then the capacitor has no losses and is ideal.

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Figure B.4: Starting from left, the ideal inductor, the high frequency model of the inductor above the typical resonance frequency ω_L , and the low frequency model for frequencies much below ω_L.

B.3 Inductor

The more realistic models of the inductor are shown in figure B.4.

The components shown in the models accounts for:

- L inductance of the inductor
- $R_s(\omega)$ ohmic resistance R due to the wire length (constant) , the skin effect, and the proximity effect.
- $C_p$capacitive effect due to the proximity of the windings.

The sketched circuit resonates at the angular frequency

$$\omega_L = \frac{1}{\sqrt{LC}} \sqrt{1 - R_s^2 \frac{C}{L}} \,.$$

For $\omega \ll \omega_L$ the capacitance becomes negligible and the inductor can be modeled as a series of an inductor with inductance L and a resistor with the ohmic resistance R.

Appendix C

Decibels

C.1 Definition of Decibel

The decibel is defined as 10 times the logarithm in base ten of a power P normalized to a reference power P_r , i.e.

$$X\ (\text{dB}) = 10 \log_{10} \frac{P}{P_r} \,. \tag{C.1}$$

Considering that

$$P = \frac{V^2}{R} = RI^2,$$

and supposing that we use the same reference resistance R_r for P, P_r,we can rewrite equ. (C.1) as

$$X\ (\text{dB}) = 20 \log_{10} \frac{V}{V_r} = 20 \log_{10} \frac{I}{I_r},$$

where V_r, and I_r are respectively the voltage and the current across the reference resistance R_r. In other words, we have to measure the voltage or the currents across equal impedaces, to get the decibels.

C.2 Generalization of the Use of Decibel

For practical purposes, the decibel is also used to report the ratio of homogeneus quantities such as the voltage output V_o over the voltage input V_i

of a two port network, or more in general the ratio of any kind of homogeneus quantities $x_1,\ x_2$

$$X\ (\text{dB}) = 20 \log_{10} \frac{x_1}{x_2}\ .$$

In this case there is no normalization respect to a reference load R_r or power P_r.

C.3 Useful Table and Properties

The next table is quite useful to easily translate decibels into magnitude

(dB)	0	1	2	3	4	5	6	7	8	9	10
Magnitude	1	1.1	1.2	1.4	1.6	1.8	2	2.2	2.5	2.8	3.2

For conveniece, let´s rewrite some useful properties of the logarithm function

$$\begin{aligned}
\log(x\, y) &= \log\ x + \log\ y, \\
\log(x/y) &= \log\ x - \log\ y, \\
\log x^n &= n \log\ x, \\
\log_a x &= \log_b x / \log_b a.
\end{aligned}$$

C.4 Standard Power References

Decibels comes in many flavors (different reference powers) depending on the application, radio frequency, microwaves, optics, et cetera.

For example the following definition is quite often used

$$X\ (\text{dBm})(R_r) = 10 \log_{10} \frac{V^2/R_r}{1\text{mW}}$$

The value of R_r depends on the application field

	$R_r(\Omega)$
Radio Frequency	50
TV Frequencies	75
Audio Frequencies	600

Appendix D

Resistor Color Code

Nominal values of resistances are coded using colors bands around the resistors (see figure below). The bands identify digits and the exponent in base ten for the resistance value and the tolerance as explained in the following table:

Band Number	1	2	3	4 (Tolerance band)	5
3 Bands	Digit	Digit	Exponent	Always 20%	
4 Bands	Digit	Digit	Exponent	Tolerance	
5 Bands	Digit	Digit	Exponent	Tolerance	Tolerance after 1000 hours

3 Band resistors have no band for the tolerance because it is assumed to be 20% of the nominal values.The fifth band is not an industry standard, but quite often it means the tolerance after 1000 hours of continuous use.

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$$R = AB \cdot 10^C, \quad \Delta R = R \cdot D$$

The bands are counted from left to right. The following table reports the coding of the values using colors and a mnemonic sentence to remember the color code table.

Mnemonic Sentence	Color	Exponent	Tolerance (%)	Tolerance (%) 5th Band
Big	Black	0	20	
Bart	Brown	1	1	1%
Rides	Red	2	2	0.1%
Over	Orange	3		0.01%
Your	Yellow	4		0.001%
Grave	Green	5		
Blasting	Blue	6		
Violent	Violet	7		
Guns	Gray	8		
Wildly.	White	9		
Go	Gold	-1	5	
Shoot (him?)	Silver	-2	10	

For example, the nominal resistance of a 4 band resistor having the sequence brown, black, orange and gold is

$$\begin{array}{r} R_{nom.} = 10\text{k}\Omega \\ \Delta R_{nom.} = 5\%10\text{k}\Omega \end{array} \quad \Rightarrow \quad R_{nom.} = (10.0 \pm 0.5)\text{k}\Omega$$

Resistor size (volume) is related to the power dissipation capability. Typical used values are 1/4W 1/2W, 1W.

Appendix E

The Cathode Ray Tube Oscilloscope

E.1 The Cathode Ray Tube Oscilloscope

The *cathode ray tube oscilloscope* is essentially an analog[1] instrument that is able to measure time varying electric signals. It is made of the following functional parts (see figure E.1):

- the cathode ray tube (CRT),
- the trigger,
- the horizontal input,
- the vertical input,
- time base generator.

Let's study in more detail each component of the oscilloscope.

E.1.1 The Cathode Ray Tube

The CRT is a vacuum envelope hosting a device called *an electron gun* , capable of producing an electron beam, whose transverse position can be modulated by two electric signals (see figures E.1 and E.7).

[1]Hybrid instruments combining the characteristics of digital and analog oscilloscopes, with a CRT, are also commercially available.

When the electron gun cathode is heated by wire resistance because of the Joule effect it emits electrons . The increasing voltage differences between a set of shaped anodes and the cathode accelerates electrons to a terminal velocity v_0 creating the so called electron beam.

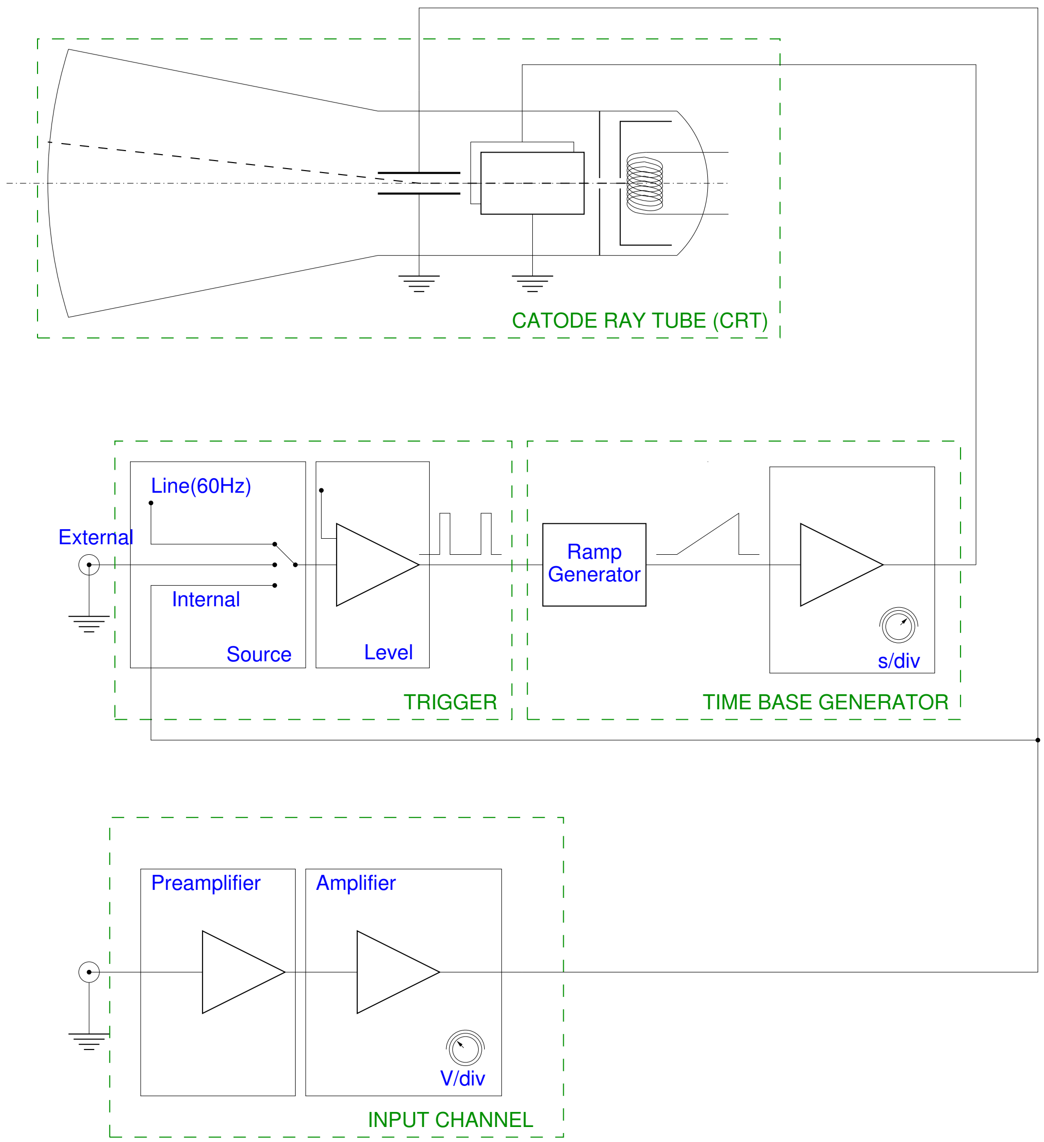

Figure E.1: Oscilloscope functional schematics

The beam then goes through two orthogonally mounted pairs of metallic plates. Applying voltage difference to those plates V_x and V_y, the beam is deflected along two orthogonal directions (x and y) perpendicular to its direction z. The deflected electrons will hit a plane screen perpendicular to the beam and coated with florescent layer. The electrons interaction with this layer generates photons, making the beam position visible on the screen.

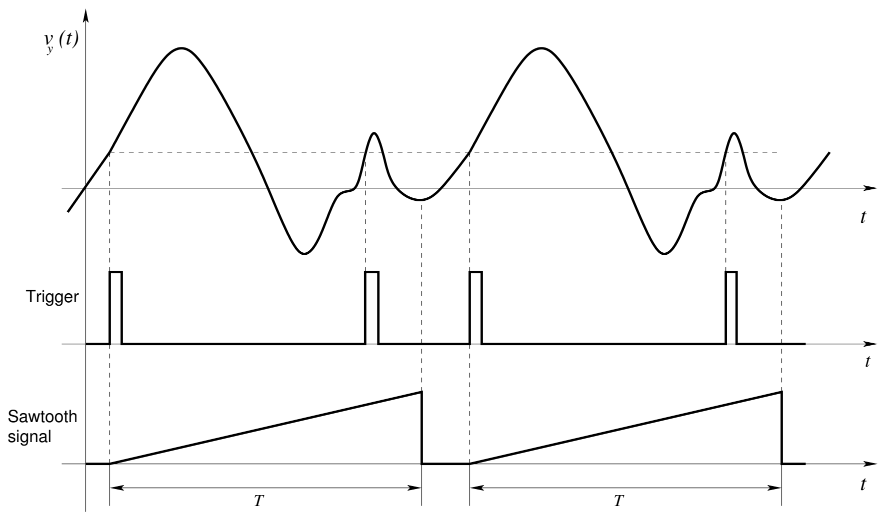

Figure E.2: Periodic Signal triggering.

E.1.2 The Horizontal and Vertical Inputs

The vertical and horizontal plates are independently driven by a variable gain amplifier to adapt the signals $v_x(t)$, and $v_y(t)$ to the screen range. A DC offset can be added to each input to position the signals on the screen. These two channels used to drive the signals to the plates signals are called horizontal and vertical inputs of the oscilloscope.

In this configuration the oscilloscope is an x-y plotter.

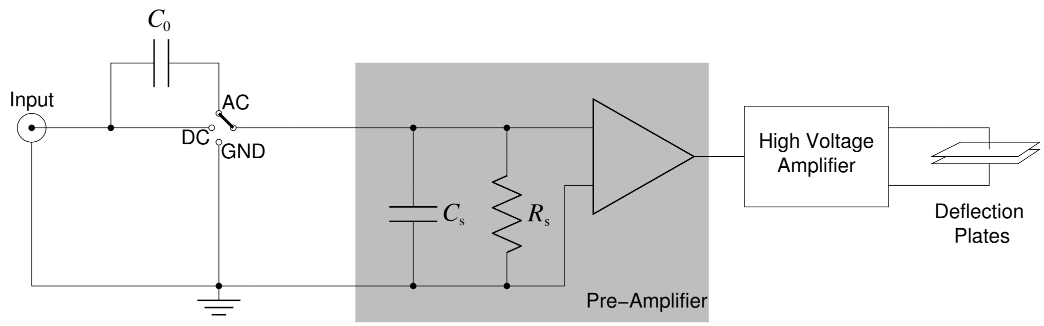

Figure E.3: Oscilloscope input impedance representation using ideal components (gray box). Input channel coupling is also shown.

E.1.3 The Time base Generator

If we apply a sawtooth signal $V_x(t) = \alpha t$ to the horizontal input, the horizontal screen axis will be proportional to time t. In this case a signal $v_y(t)$ applied to the vertical input, will depict on the oscilloscope screen the signal time evolution.

The internal ramp signal is generated by the instrument with an amplification stage that allows changes in the gain factor α and the interval of time shown on the screen. This amplification stage and the ramp generator are called the *time base generator.*

In this configuration, the horizontal input is used as a second independent vertical input, allowing the plot of the time evolution of two signals.

Visualization of signal time evolution is the most common use of an oscilloscope.

E.1.4 The Trigger

To study a periodic signal $v(t)$ with the oscilloscope, it is necessary to synchronize the horizontal ramp $V_x = \alpha t$ with the signal to obtain a steady plot of the periodic signal. The trigger is the electronic circuit which provides this function. Let's qualitatively explain its behavior.

The trigger circuit compares $v(t)$ with a constant value and produces a pulse every time the two values are equal and the signal has a given slope. The first pulse triggers the start of the sawtooth signal of period[2] T , which will linearly increase until it reaches the value $V = \alpha T$, and then is reset to zero. During this time, the pulses are ignored and the signal $v(t)$ is plotted for a duration time T. After this time, the next pulse that triggers the sawtooth signal will happen for the same previous value and slope sign of $v(t)$, and the same portion of the signal will be re-plotted on the screen.

E.2 Oscilloscope Input Impedance

A good approximation of the input impedance of the oscilloscope is shown in the circuit of figure E.3. The different input coupling modes (DC AC GND) are also represented in the circuit.

The amplifying stage is modeled using an ideal amplifier (infinite input impedance) with a resistor and a capacitor in parallel to the amplifier input.

The switch allows to ground the amplifier input and indeed to vertically set the origin of the input signal (GND position), to directly couple the input signal (DC position), or to mainly remove the DC component of the input signal (AC position).

E.3 Oscilloscope Probe

An oscilloscope probe is a device specifically designed to minimize the capacitive and resistive load added when the instrument is connected to the circuit. The price to pay is an attenuation of the signal that reaches the oscilloscope input[3].

Let's analyze the behavior of a passive probe. Figure E.4 shows the schematics of the equivalent circuit of a passive probe and of the input stage of an oscilloscope. The capacitance of the probe cable can be considered included in C_s

Considering the voltage divider equation, we have

$$H(j\omega) = \frac{V_s}{V_i} = \frac{Z_s}{Z_p + Z_s}, \tag{E.1}$$

[2]In general, the sawtooth signal period T and the period of $v(t)$ are not equal.

[3]Active probes can partially avoid this problems by amplifying the signal.

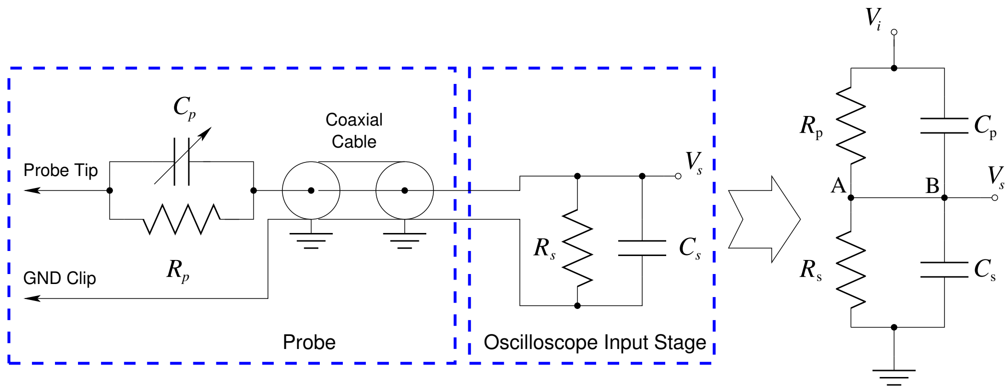

Figure E.4: Oscilloscope input stage and passive probe schematics.The equivalent circuit made of ideal components for the probe shielded cable is not shown.

where

$$\frac{1}{Z_s} = j\omega C_s + \frac{1}{R_s}, \qquad \frac{1}{Z_p} = j\omega C_p + \frac{1}{R_p},$$

and then

$$Z_s = \frac{R_s}{j\omega\tau_s + 1}, \qquad Z_p = \frac{R_p}{j\omega\tau_p + 1}.$$

Defining the following parameters

$$\tau_p = C_p R_p, \quad \alpha = \frac{R_s}{R_s + R_p}, \qquad \beta = \frac{C_p}{C_s + C_p},$$

and after some tedious algebra, equation (E.1) becomes

$$H(j\omega) = \alpha \frac{1 + j\omega\tau_p}{1 + j\omega\frac{\alpha}{\beta}\tau_p},$$

which is the transfer function from the probe input to the oscilloscope input before the ideal amplification stage.

The DC and high frequency gain of the transfer function $H(j\omega)$ are respectively

$$H(0) = \alpha, \qquad H(\infty) = \beta.$$

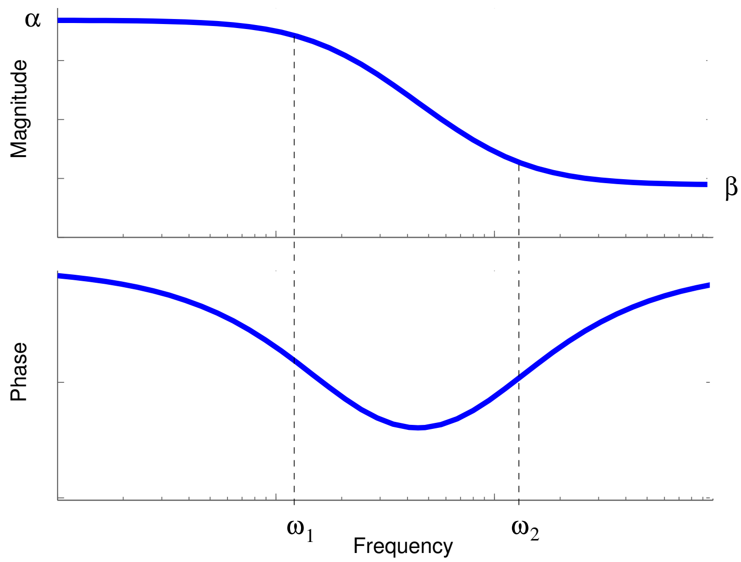

Figure E.5: Qualitative transfer function from the under compensated probe input to the oscilloscope input before the ideal amplification stage. As usual, the oscilloscope input is described having an impedance $R_s||C_s$.

The numerator and denominator of $H(j\omega)$ are respectively equal to zero, (the zeros and poles of H) when

$$\omega = \omega_z = j\frac{1}{\tau_p}, \qquad \omega = \omega_p = j\frac{\beta}{\alpha}\frac{1}{\tau_p}.$$

Figure E.5 shows the qualitative behavior of H for $\frac{\alpha}{\beta} > 1$.

E.3.1 Probe Frequency Compensation

By tuning the variable capacitor C_p of the probe, we can have three possible cases

$$\frac{\alpha}{\beta} < 1 \quad \Rightarrow \quad \text{over-compensation}$$
$$\frac{\alpha}{\beta} = 1 \quad \Rightarrow \quad \text{compensation}$$

$$\frac{\alpha}{\beta} > 1 \quad \Rightarrow \quad \text{under-compensation}$$

if $\alpha < \beta$ the transfer function attenuates more at frequencies above ω_z, and the input signal V_i is distorted.

if $\alpha = \beta$ the transfer function is constant and the input signal $V_i$will be undistorted, and attenuated by a factor α.

if $\alpha > \beta$ the transfer function attenuates more at frequencies below ω_p and the input signal $V_i$is distorted.

The ideal case is indeed the compensated case, because we will have increased the input impedance by a factor α without distorting the signal.

The probe compensation can be tuned using a signal, which shows a clear distortion when it is filtered. A square wave signal is very useful in this case because, it shows a different distortion if the probe is under or over compensated. Figure E.6 sketches the expected square wave distortion for the two un-compensated cases.

It is worthwhile to notices that

$$\frac{\alpha}{\beta} = 1, \qquad \Rightarrow \frac{R_s}{R_p} = \frac{C_p}{C_s}.$$

This condition implies that:

- the voltage difference V_1 across R_s is equal the voltage difference V_2 across C_s, i.e $V_1 = V_2$
- the voltage difference V_3 across R_p is equal the voltage difference V_4 across C_p , i.e. $V_3 = V_4$
- and indeed $V_1 + V_2 = V_3 + V_4$.

This means that no current is flowing through the branch AB, and we can consider just the resistive branch of the circuit to calculate V_s. Applying the voltage divider equation, we finally get

$$V_s = \frac{R_s}{R_s + R} V_i$$

The capacitance of the oscilloscope does not affect the oscilloscope input anymore, and the oscilloscope+probe input impedance R_i becomes greater, i.e.

$$R_i = R_s + R_p.$$

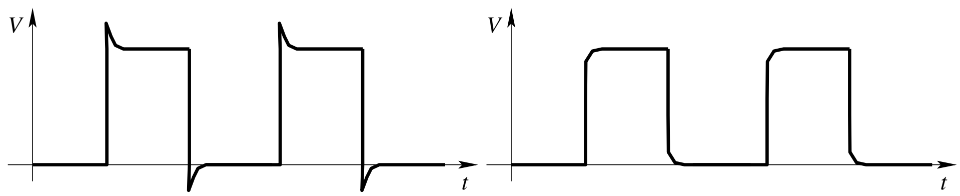

Figure E.6: Compensation of a passive probe using a square wave. Left figure shows an over compensated probe, where the low frequency content of the signal is attenuated. Right figure shows the under compensated case, where the high frequency content is attenuated.

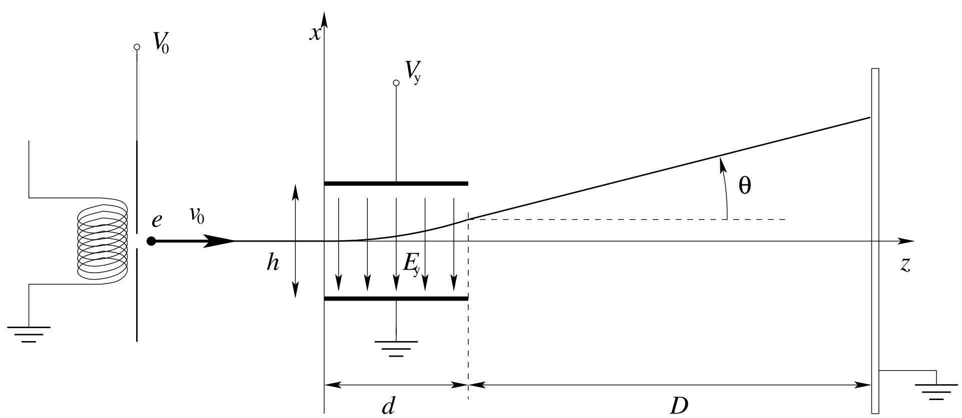

Figure E.7: CRT tube schematics. The electron enters into the electric field and makes a parabolic trajectory. After passing the electric field region it will have a vertical offset and deflection angle θ.

E.4 Beam Trajectory

Let's consider the electron motion through one pair of plates.

The electron terminal velocity v_0 coming out from the gun can be easily calculated considering that its initial potential energy is entirely converted into kinetic energy, i.e

$$\frac{1}{2}\mu v_0^2 = eV_0, \quad \Rightarrow \quad v_0 = \sqrt{2\frac{eV_0}{\mu}},$$

where μ is the electron mass, e the electron charge, and V_0 the voltage applied to the last anode.

If we apply a voltage V_y to the plates whose distance is h, the electrons will feel a force $F_y = eE_y$ due to an electric field

$$|E_y| = \frac{V_y}{h}.$$

The equation of dynamics of the electron inside the plates is

$$\begin{aligned} \mu\ddot{z} &= 0, \quad \Rightarrow \quad \dot{z} = v_0, \\ \mu\ddot{y} &= e|E_y|. \end{aligned}$$

Supposing that V_y is constant, the solution of the equation of motion will be

$$\begin{aligned} z(t) &= \sqrt{2\frac{eV_0}{\mu}}t, \\ y(t) &= \frac{1}{2}\frac{eV_y}{\mu h}t^2. \end{aligned}$$

Removing the dependency on the time t, we will obtain the electron beam trajectory , i.e.

$$y = \frac{1}{4h}\frac{V_y}{V_0}z^2,$$

which is a parabolic trajectory.

Considering that the electron is transversely accelerated until $z = d$, the total angular deflection θ will be

$$\tan\theta = \left(\frac{\partial y}{\partial z}\right)_{z=d} = \frac{1}{2}\frac{d}{h}\frac{V_y}{V_0}.$$

and displacement Y on the screen is

$$Y(V_y) = y(z = d) + \tan\theta D,$$

i.e.,

$$Y(V_y) = \frac{1}{2}\frac{d}{h}\frac{1}{V_0}(\frac{d}{2} + D)V_y.$$

Y is indeed proportional to the voltage applied to the plates through a rather complicated proportional factor.

The geometrical and electrical parameters of this proportional factor play a fundamental role in the resolution of the instrument. In fact, the smaller the distance h between the plates, or the smaller the gun voltage drop V_0, the larger is the displacement Y. Moreover, Y increases quadratically with the electron beam distance d.

E.4.1 CRT Frequency Limit

The electron transit time through the plates determine the maximum frequency that a CRT can plot. In fact, if the transit time τ is much smaller than the period T of the wave form $V(t)$, we have

$$V(t) \simeq \text{constant}, \qquad \text{if} \quad \tau \ll T,$$

and the signal is not distorted.

The transit time is

$$\tau = \frac{d}{v_0} = d\sqrt{\frac{\mu}{2eV_0}}.$$

Supposing that

$$\begin{cases} V_0 = 1\text{kV} \\ d = 20\text{mm} \\ \mu c^2 \simeq 0.5\text{MeV} \\ e = 1\text{eV} \end{cases} \qquad \Rightarrow \qquad \tau \simeq 1\text{ns}$$

Appendix F

Electromagnetic Field Noise

F.1 Introduction

Human and natural activities fill the surrounding space with electromagnetic fields (radiation) creating a very complex and unpredictable frequency spectrum of radiation. For example, domestic appliances, bulbs, fluorescent lights, and power line grids mainly irradiate at 60Hz and harmonics of 60Hz. Radios, televisions, wireless internet connections, and cellular phones networks are other typical sources, which fill the radiation spectrum from the kilohertz to the gigahertz region. Light mainly produced by the sun pervades the spectrum in the optical region. Radioactivity, gamma ray burst (GRB) emitted by astrophysical sources are for eaxmple responsible for filling the high and very high region of the spectrum.

Portion of this so complex spectrum can be attenuated by the so called electromagnetic shields but some others portions because of the energy involved cannot be effectively even attenuated.

The so called radio frequency noise can be easily attenuated (shielded) using a quite simple device known as the *Faraday cage*.

F.2 The Faraday Cage

Gauss's law states that a closed surface will prevent extern electrostatic fields from reaching the space enclosed by the surface. If the electric field is slowly varying i.e., its wavelength λ is large compared to the typical size d of the enclosure), then the field on the surface can be considered static and Gauss's law is then applicable. This enclosure is commonly called *Faraday cage.*

Using this crude approximation we can state that all frequencies much smaller than the following

$$\nu^* \sim \frac{c}{d}$$

where c is the speed of light, will be effectively attenuated. For example if $d = 1$m then the Faraday cage will attenuate the external electromagnetic fields with frequencies much smaller than $\nu^* \sim 300$MHz.

F.3 Practical Considerations

Normally, when we perform a measurement we cannot easily fit the lab in a small Faraday cage. Anyway, most of the time it is sufficient to enclose the physical system under measurement inside the cage . Then to perform the measurement we will have to connect the instrument sitting outside the cage to the system. The instruments leads acting like an antenna will still pick-up some of the ambient electromagnetic radiation. This effect can be amplified if we touch one of the leads increasing the antenna effect. A way to minimize this effect is to connect Faraday cages together. Reasonably good instruments have a built in Faraday cage connected to ground. Connecting the cages to ground will create a more or less single effective cage which will attenuate the electromagnetic noise pick-up.

Appendix G

Common Emitter BJT Amplifier

The common emitter BJT amplifier is one of the most simple design that allows to set the voltage amplification A_v quite independently from the BJT characterstic.

To properly set the BJT working point we have to forward bias the emitter base junction and reverse bias the collector base junction. But this is not enough if we want to build an amplifier. The other requirement is to set the voltage V_{CE} where the VCE characteristic is flat and wide enough to accomodate the output signal excursion. In other words, we don´t want the output to swing into the saturation region or even worst into the break down region.

The design parameters we have to fix are are I_C,V_{CE},V_{CC}, and essentially, the VCE characteristics contains all the information we need to properly bias the BJT. As last remark, voltage gain and bias point are "intimately" related and cannot be completely independent.

G.1 BJT Bias

The analysis of the circuit becomes quite easy if we observe from the V_{CE} characteristic that

$$I_C \gg I_B \tag{G.1}$$

In fact, in this case we have that $I_B$is negligible and the resistors $R_B$and $R_b$act as a simple voltage divider, i.e.

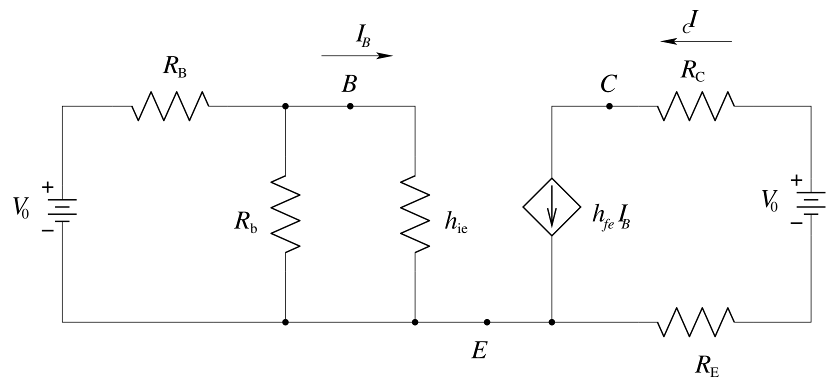

Figure G.1: Common emitter equivalent circuit which simplifies the BJT biasing

$$V_{BE} = \frac{R_b}{R_b + R_B} V_{CC} \tag{G.2}$$

The voltage difference V_{BE} must be the voltage drop of a forward polarized diode junction typically 0.7V, and this is one of the parametes we have to fulfill to properly bias the BJT. The equation G.2 set the value of one resistor as a function of the other.

The other parameter is V_{CE}. Applying the KVL to the output mesh we will have

$$V_{CE} = (R_C + R_E)\, I_C + V_{CC} \tag{G.3}$$

Equation G.2, G.3 must be satified, but they are not enough to set all the resistor values. The voltage gain will provide another constranint an set the resitor values.

G.2 BJT Gain

Using the equivalent small signal circuit model for the BJT and considering the impedance of the ideal voltage and current sources we can construct the circuit show in figure G.2. Then from that figure it is finally easy to compute the voltage gain A_v and the input and output impedance R_i and R_o of the circuit.

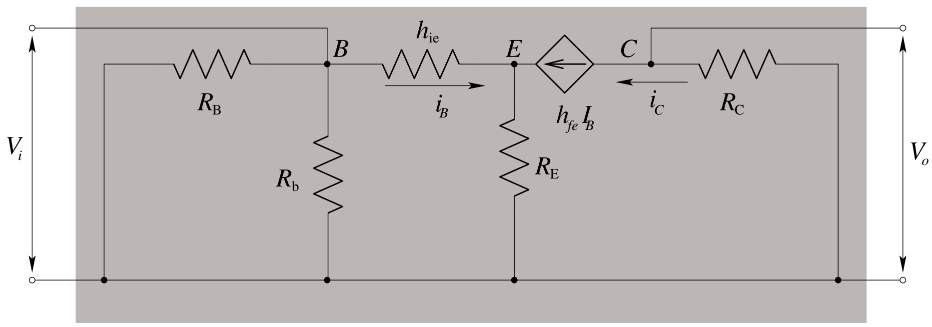

Figure G.2: Small signal circuit model for the common emitter BJT amplifier

In fact, the input and the output voltage are simply

$$\begin{cases} V_i = R_E I_E \simeq R_E I_C, \qquad (I_B \ll I_C) \\ V_o = R_C I_C \end{cases}, \qquad \Rightarrow \qquad A_v \simeq \frac{R_C}{R_E}$$

G.3 Input and Output Impedance

The input impedance is the impedance seen from the inputs lead , and can be easily computed considering that the ideal current source is an open circuit, i.e.

$$R_i = R_b || R_B || (h_{ie} + R_e)$$

The output impedance is then

$$R_o = R_C$$

G.4 Resume

Summarizing the results we have

$$\begin{aligned} V_{BE} &= \frac{R_b}{R_b + R_B} V_{CC} \\ V_{CC} &= (R_C + R_E)\, I_C + V_{CE} \\ A_v &= \frac{R_C}{R_E} \end{aligned}$$

and resolving the equation respect the unknown parameters

$$
\begin{aligned}
R_B &= R_b \left(\frac{V_{CC}}{V_{BE}} - 1 \right) \\
R_E &= \frac{V_{CC} - V_{CE}}{I_C(1 + A_v)} \\
R_C &= A_v R_E
\end{aligned}
$$

G.5 Example

Let´s set the following design values

$$
\begin{cases}
A_v &= 20 \\
V_{CC} &= 20\text{V} \\
I_C &= 10\text{mA}
\end{cases}
$$

Picking up a value for R_b and considering that to have a maximum dynamic

$$V_{CE} \simeq 10.3\text{V}$$

we finally get

$$
\begin{cases}
R_b &= 1.0\text{k}\Omega \\
R_B &= 27.5\text{k}\Omega \\
R_C &= 882\Omega \\
R_E &= 88\Omega
\end{cases}
$$